H. Contact Effects

Two substances are in electrical contact if charge carriers can pass through the interface of them. Contacts are:

1. Boundary surfaces in a crystal; for example, two-dimensional defects, grain boundaries (cf. p. 111), sudden transitions between different dopings in one and the same semiconductor ("homo-junctions" such as *pn* junctions, cf. pp. 334 ff.).
2. Interfaces between two or several substances; for example, between metal and vacuum, metal and semiconductor, or different semiconductors ("hetero-junctions"), between metal, insulator, and semiconductor ("MOS" junctions – *m*etal, *o*xide, *s*emiconductor).

The action of most electronic circuit and control elements is based on charge transport through contacts. This transport depends on the behaviour of the carrier potential energy which, in the neighbourhood of the contact, is position-dependent. One often speaks of the potential curve; the potential energy of electrons or holes is obtained from it by multiplication by $-e$ or $+e$. The basis for the explanation of a contact phenomenon is given by the band scheme in the environment of the boundary surface in the case of thermodynamic equilibrium. The potential curve will then depend only on the carrier concentrations on either side of the interface and the work functions (see below) of the substances in contact.

I. Thermodynamic Equilibrium

Thermodynamic equilibrium occurs in a crystal or between several crystals 1, 2, ... if the Fermi energy in the system considered has everywhere the same value, so that ζ in the band scheme is horizontal:

$$\zeta_1 = \zeta_2 = \ldots = \text{const.} \tag{H. 1}$$

All $\zeta_1, \zeta_2, \ldots$ must be reckoned from the same zero of the energy scale. Condition (H. 1) means, for instance, that in a crystal the net current of charge carriers of a given energy must be zero in all directions. This is possible only if

all states of the same energy have the same occupation probabilities $f(E)$, since otherwise there would exist a net particle flux in the direction of higher occupation probability.

Condition (H. 1) follows in general from thermodynamic considerations: consider two systems of particles (e.g. electrons) which are brought into contact at a temperature T. Before contact the constant volumina V_1 and V_2 contain N_1 and N_2 particles, respectively. After establishment of the contact, the particle numbers in both volumina have changed until thermodynamic equilibrium between the two volumina has been established. The condition for this process is that the free energy F of the whole system reaches a minimum value. From

$$F = F_1 + F_2 \tag{H. 2}$$

and

$$(\delta F)_{T,\,V,\,N,} = 0 \tag{H. 3}$$

we obtain

$$\delta F = \left(\frac{\partial F_1}{\partial N_1}\right)_{T,\,V_1} \delta N_1 + \left(\frac{\partial F_2}{\partial N_2}\right)_{T,\,V_2} \delta N_2 = 0. \tag{H. 4}$$

With the additional condition of a constant total number of particles

$$N_1 + N_2 = N = \text{const.} \tag{H. 5}$$

we find

$$\delta N_1 + \delta N_2 = 0. \tag{H. 6}$$

Using this we obtain from (H. 4)

$$\left(\frac{\partial F_1}{\partial N_1}\right)_{T,\,V_1} = \left(\frac{\partial F_2}{\partial N_2}\right)_{T,\,V_2}. \tag{H. 7}$$

It can be confirmed from the derivation of the Fermi–Dirac function $f(E)$ that the chemical potential (i.e. the variation of the free energy with the particle number at constant temperature and constant volume) is equal to the Fermi energy ζ:

$$\left(\frac{\partial F}{\partial N}\right)_{T,\,V} \equiv \zeta. \tag{H. 8}$$

Therefore eqn. (H. 7) can be written in the form

$$\zeta_1 = \zeta_2. \tag{H. 9}$$

In this way we have shown that the Fermi energy is horizontal also in the band scheme of a contact in thermal equilibrium.

The Fermi energy is determined with respect to the energy bands by the carrier concentration on the one hand (cf. p. 298) and, on the other hand, with respect to the vacuum potential by the work function. In general the work function for metals (cf. p. 174) as well as for semiconductors is defined as the energy difference between the Fermi level ζ and the potential energy E_∞ of an electron *in vacuo* at an infinite distance from the crystal (vacuum potential). This definition of the work function applies also to semiconductors whose Fermi level is generally unoccupied, since, for the high energies necessary for emission, the electron distribution function can be replaced by a Maxwell–Boltzmann distribution. The electron gas then behaves like a Maxwell gas of concentration n_0 [cf. eqn. (G. 19)] and potential energy ζ.

1. VOLTA POTENTIAL

Considering the band model of a contact, we choose the vacuum potential or an energy fixed to it as the zero of the energy scale. When two crystals with different work functions come into contact, the Fermi levels must get established at the same position. The carrier concentrations in the interior of the crystals are not influenced by the contact, that is, the position of the Fermi levels relative to the energy bands remains unchanged. The adjusting of the Fermi levels to the same height is thus only possible if the band schemes of the materials in contact are shifted with respect to one another. This means that

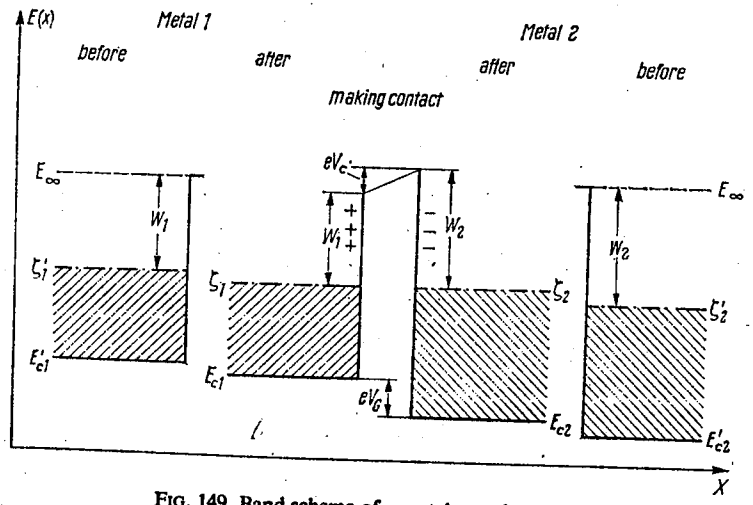

FIG. 149. Band scheme of a metal–metal contact.

in thermodynamic equilibrium a potential difference will arise between the contacting materials, whose value is equal to the difference of the work functions (cf. Fig. 149). The potential difference V_c is called the contact potential or Volta potential:

$$|V_c| = \frac{1}{e}|W_1 - W_2|. \tag{H. 10}$$

The contact potential causes an electric field whose spatial distribution depends on the carrier concentrations of the materials in contact.

In the following we shall describe the formation and the measurement of a contact potential through the example of a metal–metal contact (cf. Fig. 149). The contact is assumed to be made between the two metals 1 and 2, with the electron concentrations n_1 and n_2 and the work functions W_1 and W_2. The zero of the energy scale lies below the vacuum potential by an amount of

$$\zeta_1' + W_1 = \zeta_2' + W_2, \tag{H. 11}$$

where ζ_1', ζ_2' are the Fermi energies of the metals 1 and 2 before the contact has been made.

By analogy to (E. 24) we can neglect the temperature dependence of the Fermi energy and give the electron concentrations as

$$n_1 = \frac{1}{3\pi^2}\left[\frac{2m}{\hbar^2}(\zeta_1' - E_{c1}')\right]^{3/2}, \tag{H. 12}$$

$$n_2 = \frac{1}{3\pi^2}\left[\frac{2m}{\hbar^2}(\zeta_2' - E_{c2}')\right]^{3/2}. \tag{H. 13}$$

E_{c1}' and E_{c2}' are the energies of the bottoms of the conduction bands before contact (on p. 162 this energy was taken as the zero of the energy scale).

We assume both metals to be at the same temperature T and $W_1 < W_2$. When these two metals are brought from infinity to a small mutual distance, an exchange of electrons will set in because of the thermionic emission which always exists at $T > 0°K$; since $W_1 < W_2$, at first more electrons pass over from metal 1 to metal 2. This results in an excess of negative carriers on metal 2, an electric field is built up and a potential difference arises between the two metals. This potential difference is established at such a value that the net current between the metals is vanishing; in thermodynamic equilibrium it reaches the value V_c of the contact potential. Since no potential differences may exist in a metal, the energies of all electrons of the metals 1 and 2 are reduced by $\zeta_1' - \zeta_1$ and increased by $\zeta_2 - \zeta_2'$, respectively, and we have

$$\zeta_1' - \zeta_1 + \zeta_2 - \zeta_2' = eV_c; \tag{H. 14}$$

ζ_1 and ζ_2 are the Fermi energies of the metals 1 and 2 after the contact has been made. From this we obtain from (H. 1) and (H. 11)

$$\zeta_1' - \zeta_2' = W_2 - W_1 = eV_c . \tag{H. 15}$$

Thus, after the contact has been made, the band schemes of the initially separated metals are mutually displaced by eV_c (cf. Fig. 149). Since physically only energy differences are significant, it is common practice to take the band scheme of one of the contact materials as fixed on the common energy scale (e.g. $\zeta_1' = \zeta_1$) so that the scheme of the other is shifted by the full amount of the contact potential (e.g. $\zeta_2 - \zeta_2' = eV_c$).

The carrier exchange between the two metals which causes the contact potential involves so few particles that the concentrations n_1 and n_2 are almost uninfluenced by the contact. Thus we can write in a good approximation, according to (H. 12) and (H. 13),

$$\zeta_1' - E_{c1}' = \zeta_1 - E_{c1} \tag{H. 16}$$

and

$$\zeta_2' - E_{c2}' = \zeta_2 - E_{c2} . \tag{H. 17}$$

Taking (H. 1) into account and subtracting the above two equations, we obtain

$$E_{c2} - E_{c1} = (\zeta_1' - E_{c1}') - (\zeta_2' - E_{c2}') = \zeta_1' - \zeta_2' - (E_{c1}' - E_{c2}') \tag{H. 18}$$

or, with (H. 15),

$$eV_G \equiv E_{c2} - E_{c1} = eV_c - (E_{c1}' - E_{c2}'). \tag{H. 19}$$

The quantity V_G is called the Galvani voltage. It corresponds to the energy difference between the bottoms of the conduction bands of the contact materials. The Galvani voltage is identical with the contact potential difference only if the electron affinities of the two metals are equal; then $E_{c1}' = E_{c2}'$. The Galvani voltage cannot be measured immediately; it can be determined from eqns. (H. 12), (H. 13), and (H. 18).

In contrast to this, the contact potential can be determined directly.

2. THE KELVIN METHOD FOR THE MEASUREMENT OF THE CONTACT POTENTIAL DIFFERENCE

In principle it should be possible to measure electrostatically the contact potential difference between the two metals 1 and 2, if the two poles of the electrostatic voltmeter consist of the same metals 1 and 2 and each is connected with the same metal. The establishment of thermodynamic equilibrium is then only based on thermionic emission; at temperatures reached in practice, however, this process takes too long a time.

One uses rather a retarding field method. The two metals form the plates of a plate capacitor, which are connected through a galvanometer with a potentiometer (cf. Fig. 150). In this way the thermodynamic equilibrium and thus the contact potential difference can be established very rapidly and independently of the plate separation. As long as the voltage applied is equal to zero, a change of the plate separation gives rise to a change in charge of the capacitor and a current may flow. If an external voltage U is applied to the capacitor,

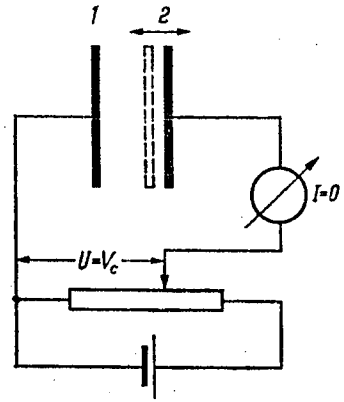

FIG. 150. Measurement of contact potential differences using the compensation method by Kelvin.

which is opposite to the contact potential difference, the charge of the two metals is reduced until it vanishes at the particular value $U = -V_c$. In this case a change of plate separation with zero charge will not give rise to a current flow. In practice the two metals 1 and 2 are used in the form of an oscillating capacitor and the alternating current is compensated by a variation of the direct voltage U. The accuracy with which the contact potential difference can be measured is $\Delta V_c \approx 10^{-4}$ V.

In the band scheme the measurement of the contact potential means the following. If $W_1 < W_2$ in thermodynamic equilibrium the metal 1 is charged positively relative to the metal 2 (cf. Fig. 149). The potential $-V_c$ of metal 2 is therefore lower than that of 1, and accordingly the potential energy eV_c of 2 is higher than that of 1 (the band scheme of 1 is assumed to be fixed, cf. p. 312). If by application of the external voltage U the potential of 2 with

respect to 1 is increased, the potential energy of 2 drops by $-eU$. If $U = -V_c$ the metals in contact have the same band schemes as the metals at infinite separation.

II. Metal–Semiconductor Contacts

Contacts involving semiconductors are in principle different from metal–metal contacts since the semiconductor may have a space charge near the boundary surface. By virtue of the Poisson equation of electrostatics

$$\frac{d^2V}{dx^2} = -\frac{1}{\varepsilon\varepsilon_0}\varrho(x) \tag{H. 20}$$

(ε is the static dielectric constant of the semiconductor and ε_0 is the vacuum permittivity), a space charge $\varrho(x)$ means the existence of a position-dependent potential and thus a position-dependent variation of the potential energy $-eV(x)$ for the electron ensemble in the semiconductor. Therefore the energy bands are shifted by $-eV(x)$ in the space charge region (the so-called bending of energy bands, band curvature). In thermodynamic equilibrium the Fermi energy remains independent of position, according to (H. 1).

1. CONTACT BETWEEN METALS AND *n*-TYPE SEMICONDUCTORS

Let us consider a contact between a metal with the work function W_m and an *n*-type semiconductor with the work function W_n (cf. Fig. 151). We assume

$$W_m > W_n \tag{H. 21}$$

and

$$W_m - W_n \ll \Delta E_i. \tag{H. 22}$$

The assumption (H. 22) makes it unnecessary to take into account the presence of the valence band. We shall also assume the band scheme of the *insulated* semiconductor to be independent of position; the bands are thus horizontal up to the semiconductor surface, that is, the donor concentration is position-independent and the surface states (cf. p. 327) are neglected.

Thermodynamic equilibrium is established if electrons pass from the semiconductor to the metal until the charge Q produced in this way gives rise to the contact potential difference $eV_c = W_m - W_n$. The positive charge of the semiconductor is constituted by the ionized donors whose electrons represent

the negative surface charge on the metal. As the distance between metal and semiconductor is reduced, the charge required by the thermodynamic equilibrium becomes higher and higher and cannot be produced any longer by the donors in the immediate vicinity of the semiconductor surface. For example, for $V_c = 10^{-1}$ V and a separation of 10^{-7} cm, the necessary charge per unit area is $Q \approx 10^{-7}$ A sec/cm^2 $\approx 10^{12}$ unit charges per cm^2. A strongly doped *n*-type semiconductor may have a donor concentration of about $N_D \approx 10^{18}$ cm^{-3}, that is, in a volume of 1 cm$^2 \times 10^{-6}$ cm at most 10^{12} ionized donors are available as positive charges. From this typical example it follows that the

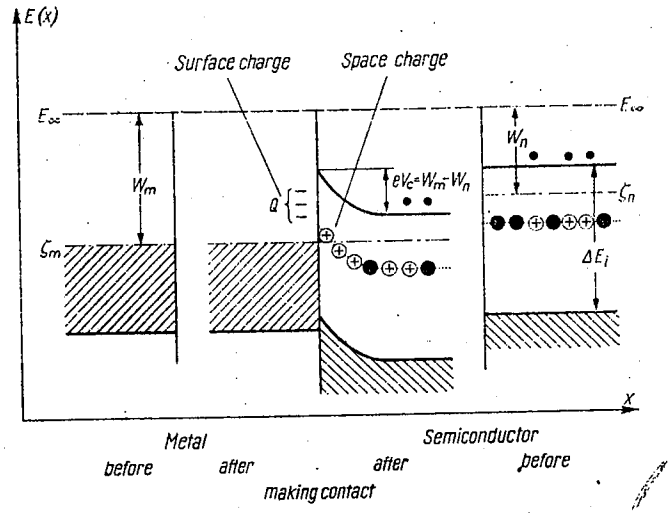

FIG. 151. Band scheme of an *n*-type semiconductor–metal contact. Band bending in the space charge region.

charge in the semiconductor must be distributed over a depth of at least 10^{-6} cm, that is, as to the order of magnitude, over at least 100 interatomic spacings. As the separation between metal and semiconductor vanishes, the surface charge of the semiconductor spreads to form a space charge.

The electric field penetrates into the semiconductor. The contact potential difference is displaced more and more into the interior of the semiconductor. The energy bands of the semiconductor become bent according to (H. 20). By virtue of the continuity condition of the dielectric displacement density the potential curve has a break at the transition from vacuum ($\varepsilon = 1$) to the semiconductor ($\varepsilon > 1$): the curved potential begins in the semiconductor with

an inclined section whose increment is smaller by the factor $1/\varepsilon$ than *in vacuo*. If the surfaces of metal and semiconductor are in contact, the entire contact potential difference lies inside the semiconductor. The energy band curvature due to this fact yields a position-dependent electron concentration $n_s(x)$ in the space charge region, in the so-called boundary layer of the semiconductor. Positive volume charge means that the energies of the states have increased compared with the Fermi level ("upward" band curvature) and the occupation probability has decreased. The boundary layer will then have a deficit of electrons; for this "depletion" layer $n_s < n$. The opposite case of an "accumulation" layer with $n_s > n$ is encountered when a negative space charge raises the occupation probability of the states in the boundary layer ("downward" band curvature).

While the position-dependent carrier concentration in the boundary layer is determined by the two contact substances, the carrier concentration in the inner part of the semiconductor has the position-independent value $n \ll N_D$ given by the condition of neutrality.

2. THE SCHOTTKY BOUNDARY LAYER

In the following we shall calculate the potential curve and the thickness of the so-called Schottky boundary layer which is characterized by a position-independent space charge density ϱ (cf. Fig. 152):

$$\varrho(x) = eN_D = \text{const.} \tag{H. 23}$$

The space charge ϱd per unit area is contained in the boundary layer of thickness d; the value of d is to be calculated. In this layer all donors are ionized and no conduction electrons are present.

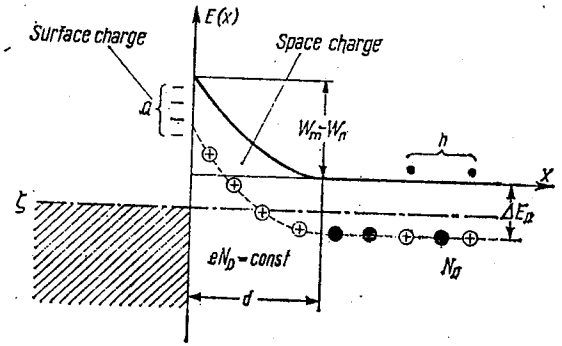

FIG. 152. Schottky layer in an *n*-type semiconductor.

The potential curve is obtained from a solution of Poisson's equation (H. 20) with the help of (H. 23):

$$\frac{d^2V}{dx^2} = -\frac{1}{\varepsilon\varepsilon_0}\varrho = -\frac{eN_D}{\varepsilon\varepsilon_0} = A. \tag{H. 24}$$

Here x is the position coordinate ($x=0$ denotes the metal–semiconductor interface, $x > 0$ is the interior of the semiconductor) and A is a constant. The solution of (H. 24) is a parabolic potential distribution in the form

$$V(x) = \frac{A}{2}x^2 + Bx + C. \tag{H. 25}$$

The constants B and C are obtained from the boundary conditions. At $x = 0$

$$-eV(0) = W_m - W_n, \tag{H. 26}$$

or

$$C = \frac{1}{e}(W_m - W_n). \tag{H. 27}$$

Then at $x = d$

$$-eV(d) = 0 \tag{H. 28}$$

and

$$\frac{dV}{dx}(d) = Ad + B = 0, \tag{H. 29}$$

that is,

$$B = -Ad. \tag{H. 30}$$

Substitution of (H. 30) in (H. 25) yields

$$V(x) = \frac{A}{2}(d-x)^2, \tag{H. 31}$$

where

$$d^2 = \frac{2C}{A} \tag{H. 32}$$

or, using (H. 24) and (H. 27),

$$V(x) = -\frac{eN_D}{2\varepsilon\varepsilon_0}(d-x)^2 \tag{H. 33}$$

and we have for the required thickness of the boundary layer

$$d = \left[\frac{2\varepsilon\varepsilon_0}{e^2N_D}(W_m - W_n)\right]^{1/2}. \tag{H. 34}$$

The thickness of this layer decreases as the donor concentration, that is, the space charge density, increases. Equation (H. 33), however, is valid only as long as the distance δ_D between the donors is much smaller than the boundary layer d, i.e. if

$$d \gg \delta_D \approx N_D^{-1/3}. \tag{H. 35}$$

For a metal-germanium contact, for example, under the assumption $W_m - W_n = 0.3$ eV, $\varepsilon_{Ge} = 16$ and $N_D = 10^{17}$ cm^{-3}, we obtain a value of $d \approx 7 \times 10^{-6}$ cm. For comparison, we have to point out that the mean distance of the donors is $\delta_D \approx 2 \times 10^{-6}$ cm so that eqn. (H. 35) is barely satisfied. This example shows that the condition must be checked in every case.

If a voltage is applied to the contact (e.g. by changing the potential of the semiconductor by $\pm U$ relative to the metal), the band scheme of the semiconductor is shifted with respect to that of the metal by $\mp eU$ (cf. Fig. 153). The

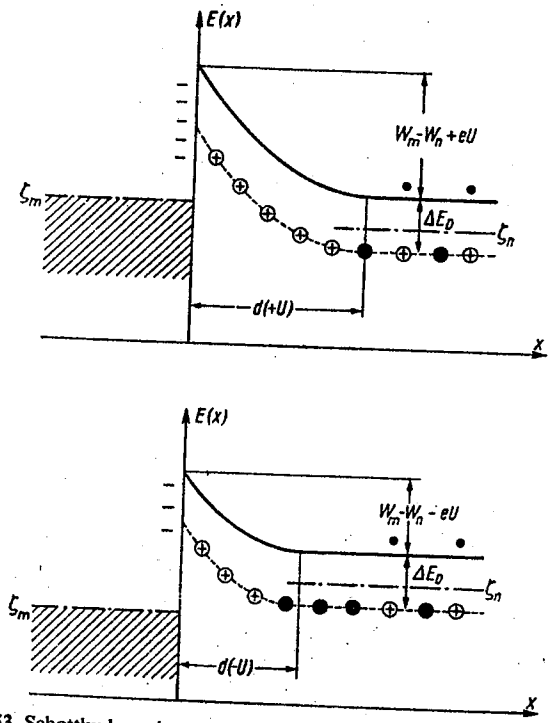

FIG. 153. Schottky layer in an n-type semiconductor with applied voltage $\pm U$.

potential curve at the contact behaves as if the work function of the metal, W_m, had been changed by $\pm eU$. The thickness of the Schottky layer is thus a function of the voltage; we have instead of (H. 34)

$$d(\pm U) = \left[\frac{2\varepsilon\varepsilon_0}{e^2 N_D}(W_m - W_n \pm eU)\right]^{1/2}. \tag{H. 36}$$

This means that with constant space charge density ϱ the space charge ϱd, which is equal to the surface charge of the metal, varies with the voltage applied.

Since, according to the assumption (H. 23), the Schottky layer contains only immobile ionized donors and no conduction electrons, it represents an insulating layer between the metal ($x \leq 0$) and the semiconductor ($x \geq d$). Electrostatically, the contact between a metal and an n-type semiconductor behaves like a capacitor whose capacity per unit area is given by

$$C = \frac{\varepsilon\varepsilon_0}{d}, \tag{H. 37}$$

or, using eqn. (H. 36), by

$$C = \left[\frac{\varepsilon\varepsilon_0 e^2 N_D}{2(\Delta W \pm eU)}\right]^{1/2}, \tag{H. 38}$$

where

$$\Delta W = W_m - W_n. \tag{H. 39}$$

We see that the capacity of the Schottky boundary layer depends on the voltage applied. Measurements of the capacitance plotted in the form of $1/C^2$ versus voltage U yield straight lines and are thus in good agreement with (H. 38). From the slope of this straight line we can determine the donor concentration or the dielectric constant of the semiconductor; the extrapolation $1/C^2 \to 0$ yields the value of ΔW. The values thus obtained for ΔW, however, are generally not in agreement with the contact potential difference $W_m - W_n$ obtained from other measurements, for instance, from determinations of the work functions W_m and W_n. This is due to the existence of surface states (cf. pp. 327 ff.) which also influence the potential curve.

3. CONTACT BETWEEN METALS AND p-TYPE SEMICONDUCTORS

The contact between a metal and a p-type semiconductor with $W_m < W_p$ can be treated in the same way as the contact between a metal and an n-type semiconductor with $W_m > W_n$. In the former case more electrons go over from the metal to the semiconductor. This results in the appearance of a negative

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FUNDEMENTALS OF SEMICONDUCTOR DEVICES
(McGRAW-HILL, 1978)

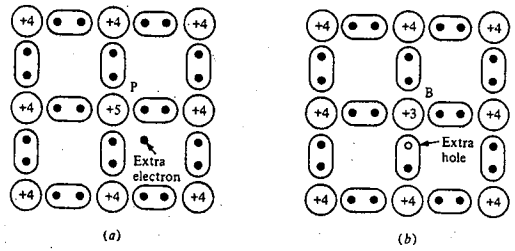

Figure 1-6 Crystal structure of silicon with a silicon atom displaced by (*a*) a pentavalent (donor) impurity atom and (*b*) a trivalent (acceptor) impurity atom.

concentration of electrons is much larger than that of holes. The conductivity of the crystal is controlled by the group V impurity concentration.

If a trivalent element, boron, aluminum, or gallium, is used as the substitutional impurity, one electron is missing from the bonding configuration, as illustrated in Fig. 1-6*b*. A hole is thus produced with a fixed negative charge remaining with the impurity atom. The number of holes is equal to the number of impurity atoms if ionization is complete. The trivalent impurity in silicon is known as an *acceptor* since it accepts an electron to produce a hole. This type of semiconductor is called *p type.*

Energy-band diagrams for both *n*- and *p*-type semiconductors are illustrated in Fig. 1-7. The energy level E_a, measured from the valence-band-edge energy E_v, is called the *ionization energy* of the acceptor impurity. The ionization energy is small because an acceptor impurity can readily accept an electron. The small ionization energy puts the impurity energy level near the valence-band edge and inside the forbidden gap. Similarly, E_d, the donor ionization energy, is measured from the band edge E_c and represents the small energy required to set the excess electron in a donor atom free. The ionization energies of some important impurities for Si, Ge, and GaAs are given in Fig. 1-8, where the levels in the lower half of the forbidden gap are

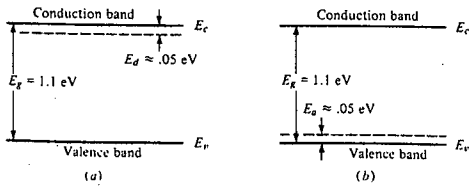

Figure 1-7 Energy-band diagram of (*a*) an *n*-type semiconductor and (*b*) a *p*-type semiconductor.

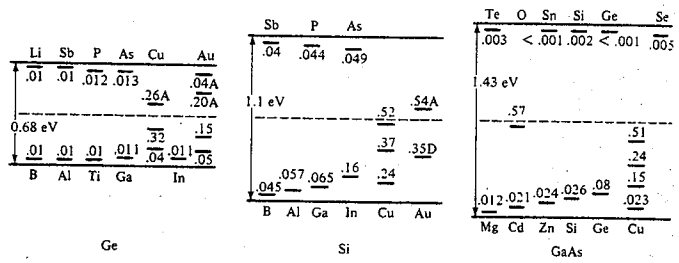

Figure 1-8 Ionization energies for various impurities in Ge, Si, and GaAs at 300 K. (*After Sze [1].*)

measured from E_v and are acceptors unless indicated by *D* for a donor level. The levels in the upper half of the forbidden gap are measured from E_c and are donors unless indicated by *A* for an acceptor level. Although most impurity atoms introduce a single energy level, interaction between host and impurity atoms may give rise to multiple impurity levels such as gold or copper in silicon.

1-4 FREE-CARRIER CONCENTRATION IN SEMICONDUCTORS

In order to determine the electrical behavior of a semiconductor, we need to know the number of electrons and holes available for current conduction. We shall consider the electron density in the conduction band and shall apply the result to holes in the valence band by analogy. The electron density in the conduction band can be obtained if the *density-of-states function* $N(E)$ and the *distribution function* $f(E)$ are given. The first function describes the available density of energy states that may be occupied by an electron. The second function tells us the probability of occupancy of these available energy states. Thus, the density of electrons is the density of occupied states in the conduction band.

Energy and Density of States

In the energy-band diagram shown in Fig. 1-9 the lowest energy level in the conduction band, i.e., the band-edge energy E_c, is the potential energy of an electron at rest. When an electron gains energy, it moves up from band edge to energy level E. In this picture, $E - E_c$ represents the kinetic energy of the electron.

The density $N(E)$ of available states as a function of energy $E - E_c$ in the

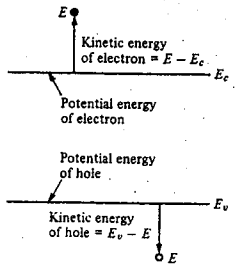

Figure 1-9 Schematic representation of kinetic and potential energy in the energy-band diagram.

conduction band is derived in Appendix A:

$$N(E) = \frac{4\pi}{h^3}(2m_e)^{3/2}(E - E_c)^{1/2} \tag{1-2}$$

where h is Planck's constant, the numerical value of which is given in Table 1-1, along with other important physical constants. The density of allowed energy states in the valence band is given by†

$$N(E) = \frac{4\pi}{h^3}(2m_h)^{3/2}(E_v - E)^{1/2} \tag{1-3}$$

Table 1-1 Physical constants

Constant	Symbol	Magnitude
Avogadro's number	N_A	6.023×10^{23} molecules/mol
Boltzmann's constant	k	1.38×10^{-23} J/K = 8.62×10^{-5} eV/K
Electronic charge	q	1.6×10^{-19} C
Electronvolt	eV	1.6×10^{-19} J
Free-electron mass	m	9.1×10^{-31} kg
Permittivity of free space	ϵ_o	8.854×10^{-14} F/cm
Permeability of free space	μ_o	1.257×10^{-8} H/cm
Planck's constant	h	6.625×10^{-34} J-s
Thermal voltage at 300 K	V_T	25.8 mV
Velocity of light	c	3×10^{10} cm/s

† Strictly speaking, m_e and m_h in Eqs. (1-2) and (1-3) are known as the density-of-state effective masses.

The valence-band-edge energy E_v represents the potential energy of the hole, and $E_v - E$ represents the kinetic energy of the hole.

The Distribution Function

The probability that an energy level E is occupied by an electron is given by the Fermi-Dirac distribution function

$$f(E) = \frac{1}{e^{(E-E_f)/kT} + 1} \tag{1-4}$$

where E_f is an important parameter called the *Fermi level*, k is Boltzmann's constant, and T is the temperature in kelvins. Figure 1-10 shows the probability function at 0, 100, 300, and 400 K. There are several interesting observations we can make regarding this figure. First, at 0 K, $f(E)$ is unity for all energy smaller than E_f. This indicates that all energy levels below E_f are occupied and all energy levels greater than E_f are empty. Second, the probability of occupancy for $T > 0$ K is always $\frac{1}{2}$ at $E = E_f$, independent of temperature. Third, the function $f(E)$ is symmetrical with respect to E_f. Thus, the probability that the energy level $E_f + dE$ is occupied equals the probability that the energy level $E_f - dE$ is unoccupied. Since $f(E)$ gives the probability that a level is occupied, the probability that a level is not occupied by an electron is

$$1 - f(E) = \frac{1}{1 + e^{(E_f - E)/kT}} \tag{1-5}$$

Since a level not occupied by an electron in the valence band means that the level is occupied by a hole, Eq. (1-5) is useful in finding the density of holes in the valence band.

For all energy levels higher than $3kT$ above E_f, the function $f(E)$ can be

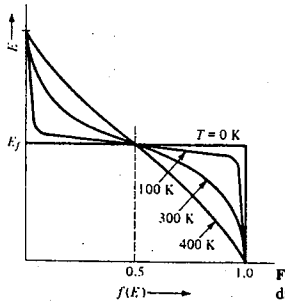

Figure 1-10 The Fermi-Dirac distribution function at different temperatures.

approximated by

$$f(E) = e^{-(E-E_f)/kT} \tag{1-6}$$

which is identical to the Maxwell-Boltzmann distribution function for classical gas particles. The electrons in the conduction band obey Eq. (1-6) if $E_c - E_f > 3kT$. For most device applications, with the exception of tunnel diodes and injection lasers, the function in Eq. (1-6) is a good approximation for $f(E)$.

Equilibrium Carrier Density

The total number of electrons in the conduction band is obtained by integrating the product of the density of states and the occupancy probability

$$n = \int_{E_c}^{\infty} f(E)N(E)\,dE \tag{1-7}$$

Substituting Eqs. (1-2) and (1-6) into Eq. (1-7) and performing the integration, we have†

$$\begin{aligned} n &= \int_{E_c}^{\infty} \frac{4\pi}{h^3}(2m_e)^{3/2}(E-E_c)^{1/2} e^{-(E-E_f)/kT}\,dE \\ &= \frac{4\pi}{h^3}(2m_e)^{3/2} e^{-(E_c-E_f)/kT} \int_{E_c}^{\infty} (E-E_c)^{1/2} e^{-(E-E_c)/kT}\,d(E-E_c) \\ &= N_c e^{-(E_c-E_f)/kT} \end{aligned} \tag{1-8}$$

where

$$N_c = 2\left(\frac{2\pi m_e kT}{h^2}\right)^{3/2} \tag{1-9}$$

The quantity N_c is called the *effective density of states in the conduction band.* In silicon, N_c is equal to $2.8 \times 10^{19}\ \text{cm}^{-3}$ at 300 K (room temperature). Similarly, the density of holes in the valence band is

$$p = \int_{-\infty}^{E_v} [1 - f(E)]N(E)\,dE \tag{1-10}$$

Substituting Eqs. (1-3) and (1-6) in Eq. (1-10) and integrating yields

$$p = N_v e^{-(E_f-E_v)/kT} \tag{1-11}$$

where

$$N_v = 2\left(\frac{2\pi m_h kT}{h^2}\right)^{3/2} \tag{1-12}$$

† Using the definite integral

$$\int_0^{\infty} x^{1/2} e^{-ax}\,dx = \frac{1}{2a}\sqrt{\frac{\pi}{a}}$$

The quantity N_v is called the *effective density of states in the valence band,* and N_v is $10^{19}\ \text{cm}^{-3}$ for silicon at room temperature. The process of obtaining the intrinsic distribution is displayed graphically in Fig. 1-11. The intrinsic-carrier density, effective density of states, and band-gap energy of Ge, Si, and GaAs at room temperature are given in Table 1-2, along with other important properties.

The product of Eqs. (1-8) and (1-11) is

$$np = N_c N_v e^{-E_g/kT} \tag{1-13}$$

where $E_g = E_c - E_v$, which is the energy of the forbidden gap. The band-gap energy is slightly temperature-dependent and can be described by the empirical relation

$$E_g = E_{go} - \beta T \tag{1-14}$$

where β is the temperature coefficient of the band-gap energy and E_{go} is the extrapolated value of E_g at 0 K. For silicon we have $E_{go} = 1.21$ eV and $\beta = 2.8 \times 10^{-4}$ eV/K. Substituting Eqs. (1-9), (1-12), and (1-14) into Eq. (1-13) and simplifying yields

$$pn = K_1 T^3 e^{-E_{go}/kT} \tag{1-15}$$

where K_1 is a constant. Equation (1-13) states that the np product is a constant in a semiconductor at a given temperature under *thermal equilibrium.* Thermal equilibrium is defined as the steady-state condition at a given temperature without external forces or excitation. This pn product depends only on the density of allowed energy states and the forbidden-gap energy, but it is independent of the impurity density or the position of the Fermi level.

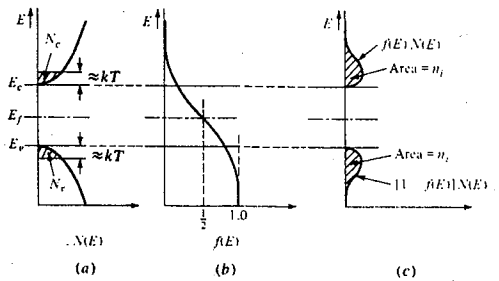

Figure 1-11 Graphical procedures for obtaining the intrinsic-carrier concentration: (*a*) the density-of-states function $N(E)$, (*b*) the Fermi-Dirac function $f(E)$, and (*c*) the density of carriers $N(E)f(E)$ at 300 K. The shaded areas in (*a*) correspond to the effective density of states; see prob. 1-11 for further explanation.

Table 1-2 Properties of Ge, Si, and GaAs at 300 K (After Sze [1] and Grove [2])

Property	Ge	Si	GaAs	SiO_2
Atoms or molecules/cm^3	4.42×10^{22}	5.0×10^{22}	2.21×10^{22}	2.3×10^{22}
Atomic or molecular weight	72.6	28.08	144.63	60.08
Density, g/cm^3	5.32	2.33	5.32	2.27
Breakdown field, V/cm	$\sim 10^5$	$\sim 3 \times 10^5$	$\sim 3.5 \times 10^5$	$\sim 6 \times 10^6$
Crystal structure	Diamond	Diamond	Zinc blende	Amorphous
Dielectric constant	16	11.8	10.9	3.9
Effective density of states				
Conduction band N_c, cm^{-3}	1.04×10^{19}	2.8×10^{19}	4.7×10^{17}	
Valence band N_v, cm^{-3}	6.1×10^{18}	1.02×10^{19}	7.0×10^{18}	
Electron affinity χ, V	4.13	4.01	4.07	0.9
Energy gap, eV	0.68	1.12	1.43	~8
Intrinsic carrier concentration n_i, cm^{-3}	2.5×10^{13}	1.5×10^{10}	10^7	
Lattice constant, Å	5.658	5.431	5.654	
Effective mass:				
Electrons	$m_e = 0.22m$, $m_e^* = 0.12m$	$m_e = 0.33m$, $m_e^* = 0.26m$	$0.068m$	
Holes	$m_h = 0.31m$, $m_h^* = 0.23m$	$m_h = 0.56m$, $m_h^* = 0.38m$	$0.56m$	
Intrinsic mobility:				
Electron, cm^2/V-s	3900	1350	8600	
Hole, cm^2/V-s	1900	480	250	
Temperature coefficient of expansion	5.8×10^{-6}	2.5×10^{-6}	5.8×10^{-6}	5×10^{-7}
Thermal conductivity, W/cm-°C	0.6	1.5	0.8	0.01

From Sze Physics of Semiconductor Devices

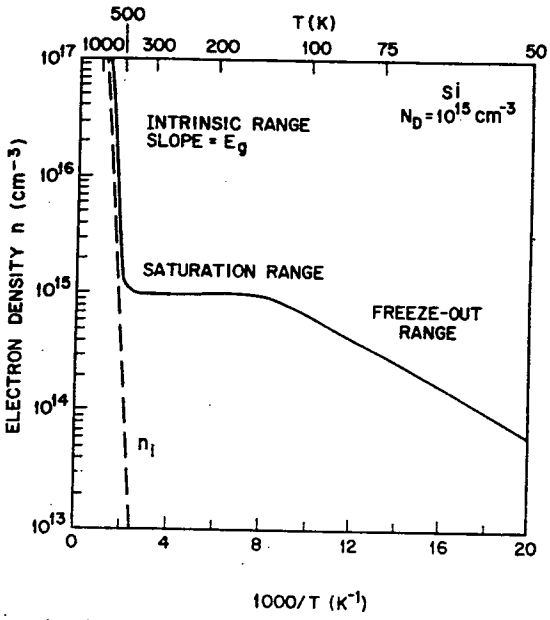

Fig. 16 Electron density as a function of temperature for a Si sample with donor impurity concentration of 10^{15} cm^{-3}. (After Smith, Ref. 5.)

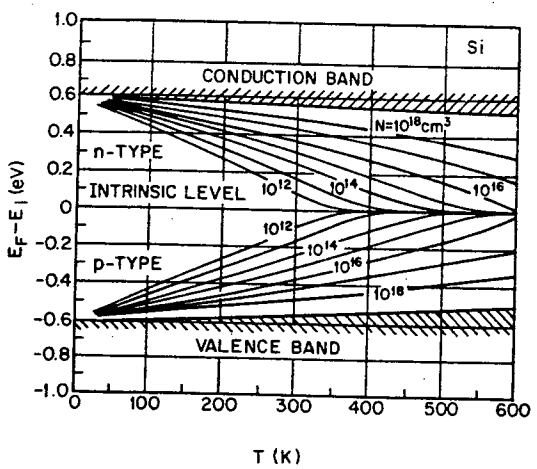

Fig. 17 Fermi level for Si as a function of temperature and impurity concentration. The dependence of the bandgap on temperature is also incorporated in the figure. (After Grove, Ref. 32.)

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1.5 CARRIER TR

1.5.1 Mobility

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The Metal-Semiconductor Junction. Schottky Diode. OHMIC CONTACTS

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Metal-to-semiconductor contacts are of great importance since they are present in every semiconductor device. They can behave either as a Schottky barrier or as an ohmic contact dependent on the characteristics of the interface. This chapter contains an analysis of the electrostatics of the M-S junction (i.e. the charge, field and potential distribution within the device) followed by a derivation of the current voltage characterisitics due to diffusion, thermionic emission and tunneling and a discussion of the non-ideal effects in Metal-Semiconductor junctions.

Structure and principle of operation

1. Structure

The structure of a metal-semiconductor junction is shown in Figure 1. It consists of a metal contacting a piece of semiconductor. An ideal Ohmic contact, a contact such that no potential exists between the metal and the semiconductor, is made to the other side of the semiconductor. The sign convention of the applied voltage and current is also shown on Figure 1.

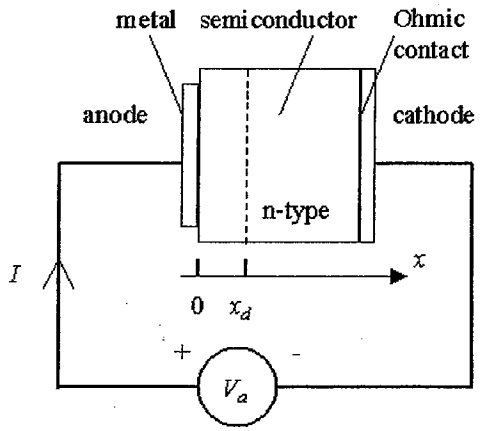


Figure 1 : Structure and sign convention of a metal-semiconductor junction

2. Flatband diagram and built-in potential

The barrier between the metal and the semiconductor can be identified on an energy band diagram. To construct such diagram we first consider the energy band diagram of the metal and the semiconductor, and align them using

the same vacuum level as shown in Figure 2 (a). As the metal and semiconductor are brought together, the Fermi energies of the metal and the semiconductor do not change right away. This yields the flatband diagram of Figure 2 (b).

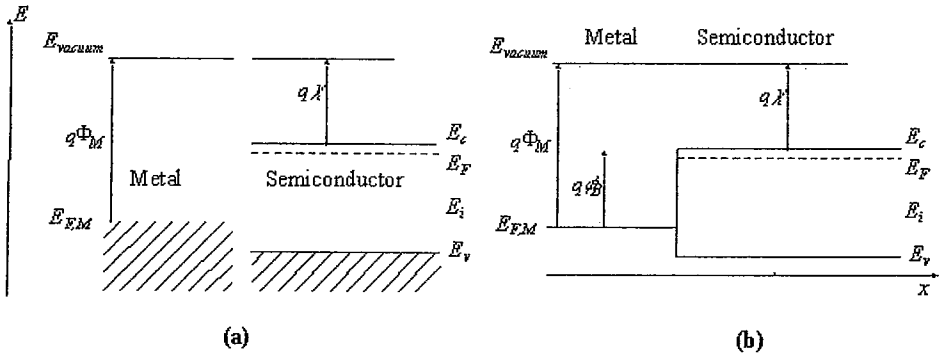


Figure 2 : Energy band diagram of the metal and the semiconductor before (a) and after (b) contact is made.

The barrier height, f_B, is defined as the potential difference between the Fermi energy of the metal and the band edge where the majority carriers reside. From Figure 2 (b) one finds that for an n-type semiconductor the barrier height is obtained from:

$$\phi_B = \Phi_M - \chi \quad \text{, for an n-type semiconductor} \tag{1.1}$$

Where F_M is the work function of the metal and c is the electron affinity. The work function of selected metals as measured in vacuum can be found in Table **1**. For p-type material, the barrier height is given by the difference between the valence band edge and the Fermi energy in the metal:

$$\phi_B = \frac{E_g}{q} + \chi - \Phi_M \quad \text{, for a p-type semiconductor} \tag{1.2}$$

A metal-semiconductor junction will therefore form a barrier for electrons and holes if the Fermi energy of the metal as drawn on the flatband diagram is somewhere between the conduction and valence band edge.

In addition, we define the built-in potential, f_I, as the difference between the Fermi energy of the metal and that of the semiconductor.

$$\phi_i = \Phi_M - \chi - \frac{E_c - E_{F,n}}{q} \quad , \quad \text{n-type} \tag{1.3}$$

$$\phi_i = \chi + \frac{E_c - E_{F,p}}{q} - \Phi_M \quad , \quad \text{p-type} \tag{1.4}$$

The measured barrier height for selected metal-semiconductor junctions is listed in Table **1**. These experimental barrier heights often differ from the ones calculated using (**1.1**) or (**1.2**). This is due to the detailed behavior of the metal-semiconductor interface. The ideal metal-semiconductor theory assumes that both materials are infinitely pure, that there is no interaction between the two materials nor is there an interfacial layer. Chemical reactions between the metal and the semiconductor alter the barrier height as do interface states at the surface of the semiconductor and interfacial layers. Some general trends however can still be observed. As predicted by (**1.1**), the barrier height on n-type semiconductors increases for metals with a higher work function as can be verified for silicon. Gallium arsenide on the other hand is known to have a large density of surface states so that the barrier height becomes virtually independent of the metal. Furthermore, one finds the barrier heights reported in the literature to vary widely due to different surface cleaning procedures.

Table 1: Workfunction of selected metals and their measured barrier height on Ge, Si and GaAs.

	Ag	Al	Au	Cr	Ni	Pt	W
Φ_M (in vacuum)	4.3	4.25	4.8	4.5	4.5	5.3	4.6
n-Ge	0.54	0.48	0.59		0.49		0.48
p-Ge	0.5		0.3				
n-Si	0.78	0.72	0.8	0.61	0.61	0.9	0.67
p-Si	0.54	0.58	0.34	0.5	0.51		0.45
n-GaAs	0.88	0.8	0.9			0.84	0.8
p-GaAs	0.63		0.42				

2.3. Thermal equilibrium

The flatband diagram, shown in Figure **2** (b), is not a thermal equilibrium diagram, since the Fermi energy in the metal differs from that in the semiconductor. Electrons in the n-type semiconductor can lower their energy by traversing the junction. As the electrons leave the semiconductor, a positive charge, due to the ionized donor atoms, stays behind. This charge creates a negative field and lowers the band edges of the semiconductor. Electrons flow into the metal until equilibrium is reached between the diffusion of electrons from the semiconductor into the metal and the drift of electrons caused by the field created by the ionized impurity atoms. This equilibrium is characterized by a constant Fermi energy throughout the structure.

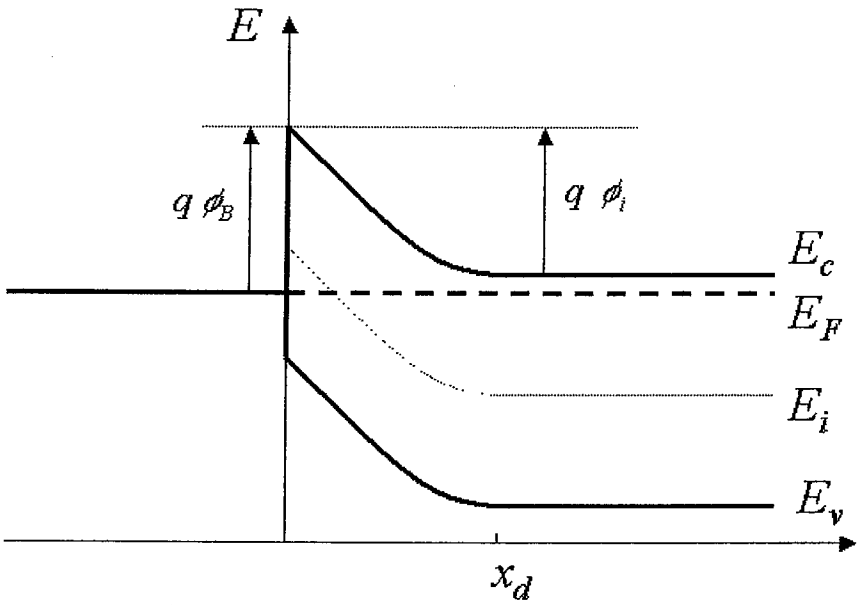


Figure 3 : Energy band diagram of a metal-semiconductor contact in thermal equilibrium.

It is of interest to note that in thermal equilibrium, i.e. with no external voltage applied, there is a region in the semiconductor close to the junction ( ), which is depleted of mobile carriers. We call this the depletion region. The potential across the semiconductor equals the built-in potential, f_i.

2.4. Forward and reverse bias

Operation of a metal-semiconductor junction under forward and reverse bias is illustrated with Figure 4. As a positive bias is applied to the metal (Figure 4 (a)), the Fermi energy of the metal is lowered with respect to the Fermi energy in the semiconductor. This results in a smaller potential drop across the semiconductor. The balance between diffusion and drift is disturbed and more electrons will diffuse towards the metal than the number drifting into the semiconductor. This leads to a positive current through the junction at a voltage comparable to the built-in potential.

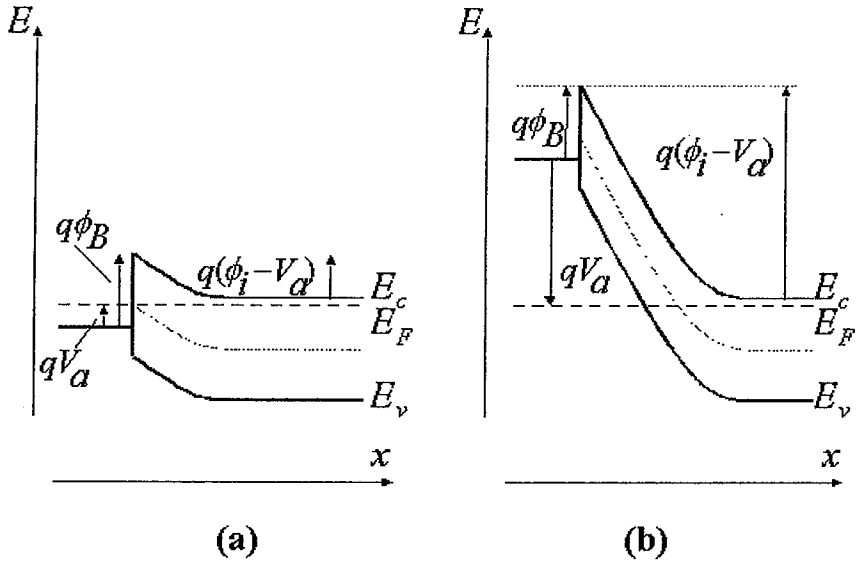


Figure 4 : Energy band diagram of a metal-semiconductor junction under (a) forward and (b) reverse bias

As a negative voltage is applied (Figure 4 (b)), the Fermi energy of the metal is raised with respect to the Fermi energy in the semiconductor. The potential across the semiconductor now increases, yielding a larger depletion region and a larger electric field at the interface. The barrier, which restricts the electrons to the metal, is unchanged so that the flow of electrons is limited by that barrier independent of the applied voltage. The metal-semiconductor junction with positive barrier height has therefore a pronounced rectifying behavior. A large current exists under forward bias, while almost no current exists under reverse bias.

The potential across the semiconductor therefore equals the built-in potential, f_i, minus the applied voltage, V_a.

$$\phi(x=\infty)-\phi(x=0)=\phi_i-V_a \qquad (2.1)$$

3. Electrostatic analysis

3.1. General discussion - Poisson's equation

The electrostatic analysis of a metal-semiconductor junction is of interest since it provides knowledge about the charge and field in the depletion region. It is also required to obtain the capacitance-voltage characteristics of the diode.

The general analysis starts by setting up Poisson's equation:

$$\frac{d^2\phi}{dx^2}=-\frac{\rho}{\varepsilon}=-\frac{q}{\varepsilon}(p-n+N_d^+-N_a^-) \qquad (3.1)$$

$$dx^{2} \qquad \varepsilon_S \qquad \varepsilon_S \qquad -$$

where the charge density, r, is written as a function of the electron density, the hole density and the donor and acceptor densities. To solve the equation, we have to express the electron and hole density, n and p, as a function of the potential, f, yielding:

$$\frac{d^2\phi}{dx^2} = \frac{2qn_i}{\varepsilon_S}\left(\sinh\frac{\phi - \phi_F}{V_t} + \sinh\frac{\phi_F}{V_t}\right) \tag{3.2}$$

with

$$\sinh\frac{\phi_F}{V_t} = \frac{N_a^- - N_d^+}{2n_i} \tag{3.3}$$

where the potential is chosen to be zero in the n-type region, where $x >> x_n$.

This second-order non-linear differential equation (3.2) can not be solved analytically. Instead we will make the simplifying assumption that the depletion region is fully depleted and that the adjacent neutral regions contain no charge. This full depletion approximation is the topic of section 3.2.

3.2. Full depletion approximation

The simple analytic model of the metal-semiconductor junction is based on the full depletion approximation. This approximation is obtained by assuming that the semiconductor is fully depleted over a distance x_d, called the depletion region. While this assumption does not provide an accurate charge distribution, it does provide very reasonable approximate expressions for the electric field and potential throughout the semiconductor.

3.3. Full depletion analysis

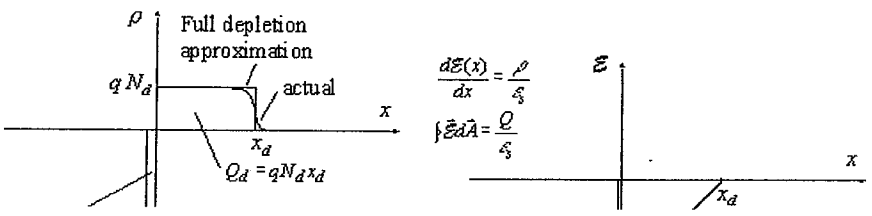
We now apply the full depletion approximation to an M-S junction containing an n-type semiconductor. We define the depletion region to be between the metal-semiconductor interface ($x = 0$) and the edge of the depletion region ($x = x_d$). The depletion layer width, x_d, is unknown at this point but will later be expressed as a function of the applied voltage.

To find the depletion layer width, we start with the charge density in the semiconductor and calculate the electric field and the potential across the semiconductor as a function of the depletion layer width. We then solve for the depletion layer width by requiring the potential across the semiconductor to equal the difference between the built-in potential and the applied voltage, $f_i - V_a$. The different steps of the analysis are illustrated by Figure 3.1.

As the semiconductor is depleted of mobile carriers within the depletion region, the charge density in that region is due to the ionized donors. Outside the depletion region, the semiconductor is assumed neutral. This yields the following expressions for the charge density, r:

$$\begin{aligned} \rho(x) &= qN_d \qquad 0 < x < x_d \\ \rho(x) &= 0 \qquad\quad x_d < x \end{aligned} \tag{3.3.4}$$

where we assumed full ionization so that the ionized donor density equals the donor density, N_d. This charge density is shown in Figure 3.1 (a). The charge in the semiconductor is exactly balanced by the charge in the metal, Q_M, so that no electric field exists except around the metal-semiconductor interface.



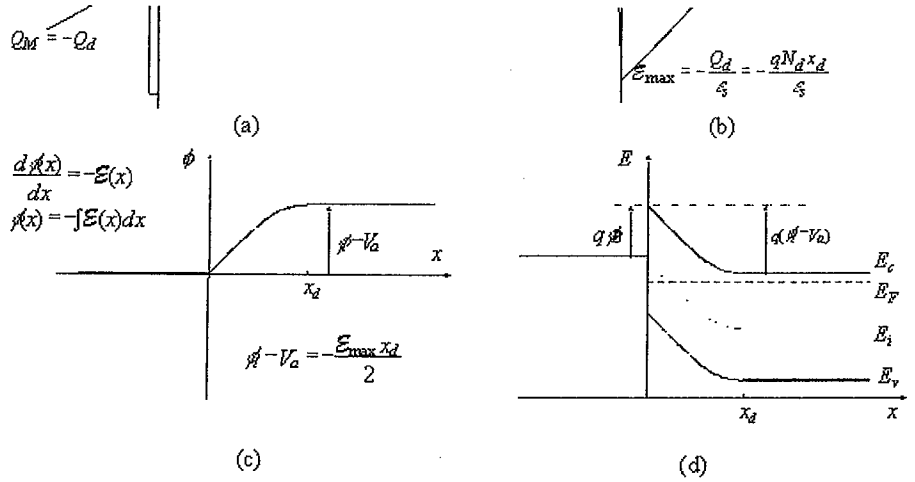


Figure 3.1 : (a) Charge density, (b) electric field, (c) potential and (d) energy as obtained with the full depletion analysis.

Using Gauss's law we obtain electric field as a function of position, also shown in Figure 3.1 (b):

$$\begin{aligned} \mathcal{E}(x) &= -\frac{qN_d}{\varepsilon_s}(x_d - x) \qquad 0 < x < x_d \\ \mathcal{E}(x) &= 0 \qquad\qquad\qquad\quad x_d \le x \end{aligned} \tag{3.5}$$

where e_s is the dielectric constant of the semiconductor. We also assumed that the electric field is zero outside the depletion region. It is expected to be zero there since a non-zero field would cause the mobile carriers to redistribute until there is no field. The depletion region does not contain mobile carriers so that there can be an electric field. The largest (absolute) value of the electric field is obtained at the interface and is given by:

$$\mathcal{E}(x=0) = -\frac{qN_d x_d}{\varepsilon_s} = -\frac{Q_d}{\varepsilon_s} \tag{3.6}$$

where the electric field was also related to the total charge (per unit area), Q_d, in the depletion layer. Since the electric field is minus the gradient of the potential, one obtains the potential by integrating the expression for the electric field, yielding:

$$\begin{aligned} \phi(x) &= 0 \qquad\qquad\qquad\qquad x \le 0 \\ \phi(x) &= \frac{qN_d}{2\varepsilon_s}[x_d^2 - (x_d - x)^2] \qquad 0 < x < x_d \\ \phi(x) &= \frac{qN_d x_d^2}{2\varepsilon_s} \qquad\qquad\qquad x_d \le x \end{aligned} \tag{3.7}$$

We now assume that the potential across the metal can be neglected. Since the density of free carriers is very high in a metal, the thickness of the charge layer in the metal is very thin. Therefore, the potential across the metal is several orders of magnitude smaller that that across the semiconductor, even though the total amount of charge is the same in both regions.

The total potential difference across the semiconductor equals the built-in potential, f_i, in thermal equilibrium and is further reduced/increased by the applied voltage when a positive/negative voltage is applied to the metal as described by equation (3.2.5). This boundary condition provides the following relation between the semiconductor potential at the surface, the applied voltage and the depletion layer width:

$$\phi - V_a = -\phi(x=0) = \frac{qN_d x_d^2}{} \tag{3.8}$$

$2\varepsilon_s$

Solving this expression for the depletion layer width, x_d, yields:

$$x_d = \sqrt{\frac{2\varepsilon_s(\phi_i - V_a)}{qN_d}} \tag{3.9}$$

3.4. Junction capacitance

In addition, we can obtain the capacitance as a function of the applied voltage by taking the derivative of the charge with respect to the applied voltage yielding:

$$C_j = \left|\frac{dQ_d}{dV_a}\right| = \sqrt{\frac{q\varepsilon_s N_d}{2(\phi_i - V_a)}} = \frac{\varepsilon_s}{x_d} \tag{3.10}$$

The last term in the equation indicates that the expression of a parallel plate capacitor still applies. One can understand this once one realizes that the charge added/removed from the depletion layer as one decreases/increases the applied voltage is added/removed only at the edge of the depletion region. While the parallel plate capacitor expression seems to imply that the capacitance is constant, the metal-semiconductor junction capacitance is not constant since the depletion layer width, x_d, varies with the applied voltage.

3.5. Schottky barrier lowering

Image charges build up in the metal electrode of a metal-semiconductor junction as carriers approach the metal-semiconductor interface. The potential associated with these charges reduces the effective barrier height. This barrier reduction tends to be rather small compared to the barrier height itself. Nevertheless this barrier reduction is of interest since it depends on the applied voltage and leads to a voltage dependence of the reverse bias current. Note that this barrier lowering is only experienced by a carrier while approaching the interface and will therefore not be noticeable in a capacitance-voltage measurement.

An energy band diagram of an n-type silicon Schottky barrier including the barrier lowering is shown in Figure 3.2:

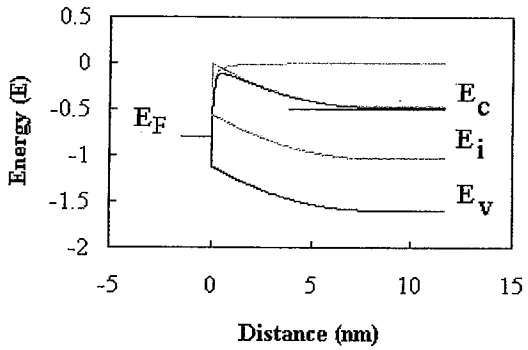


Figure 3.2: Energy band diagram of a silicon Schottky barrier with $f_B = 0.8$ V and $N_d = 10^{19}$ cm^{-3}.

Shown is the energy band diagram obtained using the full-depletion approximation, the potential reduction experienced by electrons, which approach the interface and the resulting conduction band edge. A rounding of the conduction band edge can be observed at the metal-semiconductor interface as well as a reduction of the height of the barrier.

The calculation of the barrier reduction assumes that the charge of an electron close to the metal-semiconductor interface attracts an opposite surface charge, which exactly balances the electron's charge so that the electric field

surrounding the electron does not penetrate beyond this surface charge. The time to build-up the surface charge and the time to polarize the semiconductor around the moving electron is assumed to be much shorter than the transit time of the electron . This scenario is based on the assumption that there are no mobile or fixed charges around the electron as it approaches the metal-semiconductor interface. The electron and the induced surface charges are shown in Figure 3.3:

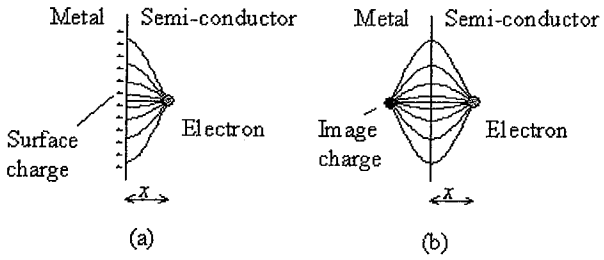


Figure 3.3: a) Field lines and surface charges due to an electron in close proximity to a perfect conductor and b) the field lines and image charge of an electron.

It can be shown that the electric field in the semiconductor is identical to that of the carrier itself and another carrier with opposite charge at equal distance but on the opposite side of the interface. This charge is called the image charge. The difference between the actual surface charges and the image charge is that the fields in the metal are distinctly different. The image charge concepts is justified on the basis that the electric field lines are perpendicular to the surface a perfect conductor, so that, in the case of a flat interface, the mirror image of the field lines provides continuous field lines across the interface.

The barrier lowering depends on the square root of the electric field at the interface and is calculated from:

$$\Delta\phi_B = \sqrt{\frac{q\mathcal{E}_{max}}{4\pi\varepsilon_s}} \tag{3.11}$$

4. Schottky diode current

The current across a metal-semiconductor junction is mainly due to majority carriers. Three distinctly different mechanisms exist: diffusion of carriers from the semiconductor into the metal, thermionic emission of carriers across the Schottky barrier and quantum-mechanical tunneling through the barrier. The diffusion theory assumes that the driving force is distributed over the length of the depletion layer. The thermionic emission theory on the other hand postulates that only energetic carriers, those, which have an energy equal to or larger than the conduction band energy at the metal-semiconductor interface, contribute to the current flow. Quantum-mechanical tunneling through the barrier takes into account the wave-nature of the electrons, allowing them to penetrate through thin barriers. In a given junction, a combination of all three mechanisms could exist. However, typically one finds that only one limits the current, making it the dominant current mechanism.

The analysis reveals that the diffusion and thermionic emission currents can be written in the following form:

$$J_n = qvN_c \exp(-\frac{\phi_B}{V_t})\left[\exp(\frac{V_a}{V_t}) - 1\right] \tag{4.1}$$

This expression states that the current is the product of the electronic charge, q, a velocity, v, and the density of available carriers in the semiconductor located next to the interface. The velocity equals the mobility multiplied with the field at the interface for the diffusion current and the Richardson velocity (see section **3.4.2**) for the thermionic emission current. The minus one term ensures that the current is zero if no voltage is applied as in thermal equilibrium any motion of carriers is balanced by a motion of carriers in the opposite direction.

The tunneling current is of a similar form, namely:

$$J_n = q v_R n \Theta \tag{4.2}$$

where v_R is the Richardson velocity and n is the density of carriers in the semiconductor. The tunneling probability term, Q, is added since the total current depends on the carrier flux arriving at the tunnel barrier multiplied with the probability, Q, that they tunnel through the barrier.

4.1. Diffusion current

This analysis assumes that the depletion layer is large compared to the mean free path, so that the concepts of drift and diffusion are valid. The resulting current density equals:

$$J_n = \frac{q^2 D_n N_c}{V_t}\sqrt{\frac{2q(\phi_i - V_a)N_d}{\varepsilon_s}}\exp(-\frac{\phi_B}{V_t})[\exp(\frac{V_a}{V_t}) - 1] \quad (4.3)$$

The current therefore depends exponentially on the applied voltage, V_a, and the barrier height, f_B. The prefactor can more easily be understood if one rewrites it as a function of the electric field at the metal-semiconductor interface, $\mathcal{E}_{max}$:

$$\mathcal{E}_{max} = \sqrt{\frac{2q(\phi_i - V_a)N_d}{\varepsilon_s}} \quad (4.4)$$

yielding:

$$J_n = q\mu_n \mathcal{E}_{max} N_c \exp(-\frac{\phi_B}{V_t})[\exp(\frac{V_a}{V_t}) - 1] \quad (4.5)$$

so that the prefactor equals the drift current at the metal-semiconductor interface, which for zero

4.2 Thermionic emission

The thermionic emission theory assumes that electrons, which have an energy larger than the top of the barrier, will cross the barrier provided they move towards the barrier. The actual shape of the barrier is hereby ignored. The current can be expressed as:

$$J_{MS} = A^* T^2 e^{-\phi_B / V_t}(e^{V_a / V_t} - 1) \quad (4.6)$$

where $A^* = \frac{4\pi q m^* k^2}{h^3}$ is the Richardson constant and f_B is the Schottky barrier height.

The expression for the current due to thermionic emission can also be written as a function of the average velocity with which the electrons at the interface approach the barrier. This velocity is referred to as the Richardson velocity given by:

$$v_R = \sqrt{\frac{kT}{2\pi m}} \quad (4.7)$$

So that the current density becomes:

$$J_n = q v_R N_c \exp(-\frac{\phi_B}{V_t})[\exp(\frac{V_a}{V_t}) - 1] \quad (4.8)$$

4.3. Tunneling

The tunneling current is obtained from the product of the carrier charge, velocity and density. The velocity equals the Richardson velocity, the velocity with which on average the carriers approach the barrier. The carrier density equals the density of available electrons, n, multiplied with the tunneling probability, Q, yielding:

$$J_n = q v_R n \Theta \quad (4.9)$$

Where the tunneling probability is obtained from:

$$\Theta = \exp\left(-\frac{4}{3}\frac{\sqrt{2qm^*}}{\hbar}\frac{\phi_B^{3/2}}{\mathcal{E}}\right) \qquad (4.10)$$

and the electric field equals $\mathcal{E} = f_B/L$.

The tunneling current therefore depends exponentially on the barrier height, f_B, to the 3/2 power.

Bibliography

1. Physics of Semiconductor Devices, Second edition, S. M. Sze, Wiley & Sons, 1981, Chapter 5.
2. Device Electronics for Integrated Circuits, Second edition, R.S. Muller and T. I. Kamins, Wiley & Sons, 1986, Chapter 3.

SCHOTTKY DIODES

Metal-semiconductor contact at zero bias

Electrons in the conduction band of a crystal can be viewed as sitting in a potential box formed by the crystal boundaries (see Fig. 1). This potential box for electrons is usually deeper in a metal than in a semiconductor. If a metal and a semiconductor are brought together into a close proximity, some electrons from the metal will move into the semiconductor and some electrons from the semiconductor will move into the metal. However, since the barrier for the electron escape from the metal is higher, more electrons will transfer from the semiconductor into the metal than in the opposite direction. At thermal equilibrium, the metal will be charged negatively, and the semiconductor will be charged positively, forming a dipole layer that is very similar to that in a p^+-n junction. The Fermi level will be constant throughout the entire metal-semiconductor system, and the energy band diagram in the semiconductor will be similar to that for an n-type semiconductor in a p^+-n junction (see Fig. 2).

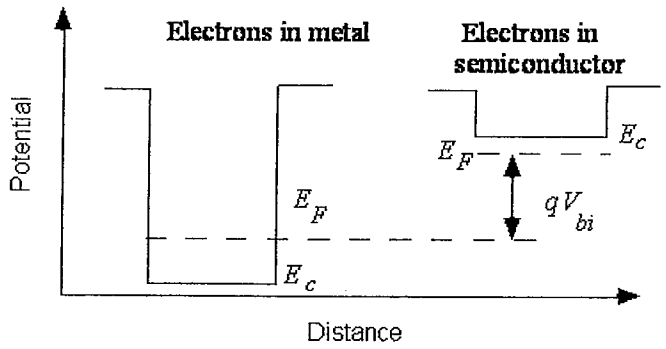
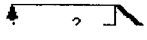


Fig. 1. Schematic energy diagram for electrons in conduction bands of a metal and of a semiconductor.

Energies F_m and F_S shown in Fig. 2 are called the metal and the semiconductor **work functions**. The **work function** is equal to the difference between the **vacuum level** (which is defined as a free electron energy in vacuum) and the Fermi level. The **electron affinity** of the semiconductor, C_S (also shown in Fig. 2), corresponds to the energy separation between the vacuum level and the conduction band edge of the semiconductor.



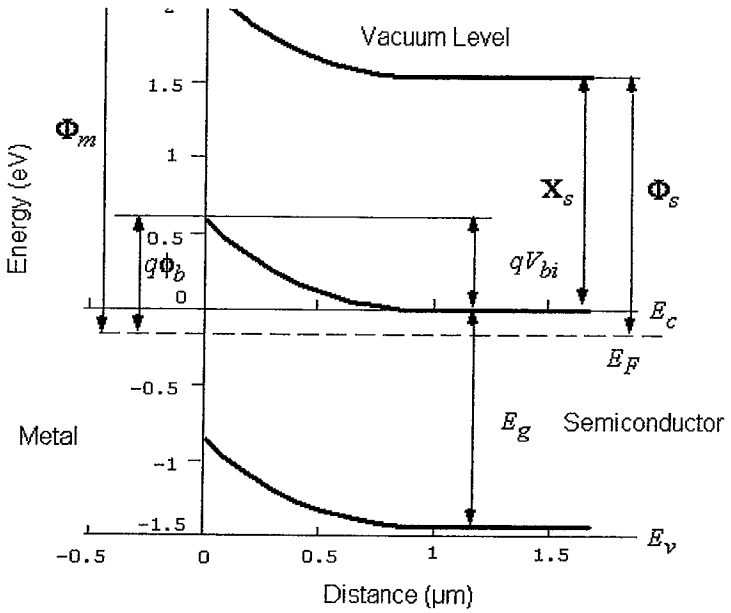


Fig. 2. Simplified energy diagram of GaAs metal-semiconductor barrier $q\,f_b$ is the barrier height (0.75 eV), C_s is the electron affinity in the semiconductor, F_s and F_m are the semiconductor and the metal work functions, and V_{bi} (0.591 V) is the built-in voltage. Donor concentration in GaAs is 10^{15} cm^{-3}.

A metal-semiconductor diode is called a **Schottky diode**. In the idealized picture of the Schottky junction shown in Fig. 2, the energy barrier between the semiconductor and the metal is

$$q\phi_b = \Phi_m - \mathbf{X}_s \qquad (1)$$

Since $F_m > F_s$ the metal is charged negatively. The positive net space charge in the semiconductor leads to a band bending

$$qV_{bi} = \Phi_m - \Phi_s \qquad (2)$$

where V_{bi} is called the **built-in voltage**, in analogy with the corresponding quantity in a *p-n* junction. Note that qV_{bi} is also identical to the difference between the Fermi levels in the metal and the semiconductor when separated by a large distance (no exchange of charge); see Fig. 1.

However, eq. (1) and Fig. 2 are not quite correct. In reality, a change in the metal work function, F_m, is not equal to the corresponding change in the barrier height ,f_b, as predicted by eq. (1). In actual Schottky diodes, f_b increases with an increase in F_m but only by 0.1 to 0.3 eV when F_m increases by 1 to 2 eV. Even though a detailed and accurate understanding of Schottky barrier formation remains a challenge, many properties of Schottky barriers may be understood independently of the exact mechanism determining the barrier height. In other words, we can simply determine the effective barrier height from experimental data. Usually, as a crude and empirical rule of thumb, we can assume that the Schottky barrier height for an *n*-type semiconductor is close to 1/2 and 2/3 of the energy gap.

In a Schottky diode, the semiconductor band diagram looks very similar to that of an *n*-type semiconductor in a p^+-*n* diode (compare Fig. 1a and 2). Hence, the variation of the space charge density, r, the electric field, *F*, and the potential, f, in the semiconductor near the

metal-semiconductor interface can be found using the depletion approximation:

$$R_c = \frac{\rho_c}{S} \quad (3)$$

$$R_c = \frac{R_{cm}}{W} \quad (4)$$

$$R_{n,n+1} = 2R_c + R_{sq}\frac{L_{n,n+1}}{W} \quad (5)$$

(Here $x = 0$ corresponds to the metal-semiconductor interface.) The depletion layer width, x_n, at zero bias is given by

$$R_{sq} = \frac{1}{\sigma t} \quad (6)$$

Schottky diode under bias

Forward bias corresponds to a positive voltage applied to the metal with respect to the semiconductor. Just as for a p^+-n junction, the depletion width under small forward bias and reverse bias may be obtained by substituting V_{bi} with $V_{bi} - V$, where V is the applied voltage. As illustrated in Fig. 3, the application of a forward bias decreases the potential barrier for electrons moving from the semiconductor into the metal. Hence, the current-voltage characteristic of a Schottky diode can be described by a **diode equation**, similar to that for a p-n junction diode :

$$I = I_s\left[\exp\left(\frac{V - IR_s}{\eta V_{th}}\right) - 1\right] \quad (7)$$

where I_s is the saturation current, R_s is the series resistance, $V_{th} = k_B T/q$ is the thermal voltage, and η is the ideality factor (η typically varies from 1.02 to 1.6).

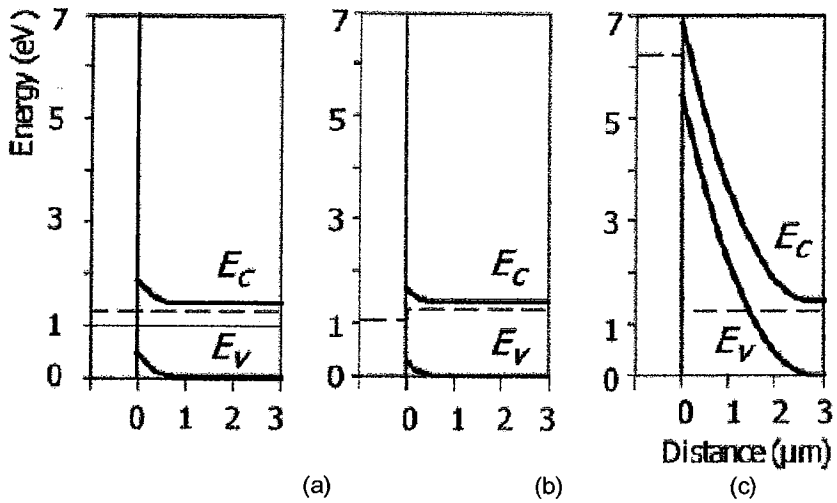


Fig. 3. Band diagrams for a GaAs Schottky barrier diode at (a) zero bias, (b) 0.2 V forward bias, and (c) 5 V reverse bias. Dashed line shows the position of the Fermi level in the metal ($x < 0$) and

in the semiconductor ($x > 0$).

Thermionic emission.

The diode saturation current, I_s, is typically much larger for Schottky barrier diodes than in *p-n* junction diodes since the Schottky barrier height is smaller than the barrier height in *p-n* junction diodes. In a *p-n* junction, the height of the barrier separating electrons in the conduction band of the *n*-type region from the bottom of the conduction band in the *p*-region is on the order of the energy gap. A typical Schottky barrier height is only about two thirds of the energy gap or less, as mentioned above. Also, the mechanism of the electron conduction is different. One can show that the saturation current density in a Schottky diode with a relatively low doped semiconductor is given by

$$j_{ss} = A^* T^2 \exp\left(-\frac{\phi_b}{k_B T}\right) \qquad (8)$$

where A^* is called the Richardson constant. For a conduction band minimum with spherical surfaces of equal energy (such as the G minimum in GaAs),

$$A^* = \alpha \frac{m_n q k_B^2}{2\pi^2 \hbar^3} \approx 120\, \alpha \frac{m_n}{m_e} \left(\frac{\mathrm{A}}{\mathrm{cm^2 K^2}}\right) \qquad (9)$$

where m_n is the effective mass and a is an empirical factor on the order of unity. The Schottky diode model described by eqs. (8) and (9) is called the **thermionic emission model**. For Schottky barrier diodes of Si, A^* = 96 A/(cm^{2}K^2). For GaAs, A^* = 4.4 A/(cm^{2}K^2).

The basic assumption of the thermionic model is that electrons have to pass over the barrier in order to cross the boundary between the metal and the semiconductor. Hence, to find the saturation current, we have to estimate the number of electrons passing over the barrier and their velocities. The number of electrons, $N(E)dE$, having energies between E and $E + dE$ is proportional to the product of the Fermi-Dirac distribution function, $f(E)$, and the number of states in this energy interval, $g(E)dE$, where $g(E)$ is the density of states:

$$N(E)dE = g(E) f(E) dE \qquad (10)$$

[$N(E) = dn(E)dE$ where $n(E)$ is the number of electrons in the conduction band with energies higher than E. At high energies, the Fermi-Dirac occupation function is very close to the Boltzmann distribution function :

$$f_n(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)} \approx \exp\left(\frac{E_F - E}{k_B T}\right) \qquad (11)$$

The next step should be to multiply the number of the electrons, $N(E)dE$, in the energy interval from E to $E + dE$ by the velocity of these electrons. We have to account for different directions of the electron velocities and integrate over energies higher than the barrier height in order to determine the flux of the electrons coming from the semiconductor into the metal. Finally, we deduct the flux of the electrons coming from the metal into the semiconductor. The difference between these two fluxes will be proportional to the current density predicted by the thermionic model. However, we can take a much simpler route if we are interested in understanding the physics of the thermionic model. To this end, let us consider a Schottky diode under a strong reverse bias when V is negative and $-V >> hk_BT$. Then $I = -I_s$ [see eq. (7)], and the band diagram looks like that shown

in Fig. 3c. In this case the energy difference between the Fermi level in the semiconductor and the top of the barrier is so large that practically no electrons are available to come from the semiconductor into the metal. However, the Fermi level in the metal is much closer to the top of the barrier, and electrons still come from the metal into the semiconductor. The flux of these electrons constitutes the saturation current. In order to estimate this flux, we should recall that the density of states is a relatively slow function of energy [$g(E)$ is proportional to $(E-E_c)^{1/2}$; compared to the distribution function, which decreases by exp(1) Ω2.718 each time E increases by k_BT. Hence, the largest contribution into the electron flux will come from the electrons that are a few k_BT above the barrier. The number of such electrons will be proportional to the effective density of states in the semiconductor

$$N_c = 2\left(\frac{m_n k_B T}{2\pi\hbar^2}\right)^{3/2} \tag{12}$$

and to exp(–f$_b$/k_BT). Their velocity in the direction perpendicular to the metal semiconductor interface is proportional to the thermal velocity

$$v_{thnx} = \sqrt{\frac{k_B T}{m_n}} \tag{13}$$

Hence, the saturation current density is given by

$$j_{ss} = CqN_c \exp\left(-\frac{\phi_b}{k_B T}\right) v_{thnx} = 2C\left(\frac{m_n k_B T}{2\pi\hbar^2}\right)^{3/2} \sqrt{\frac{k_B T}{m_n}} \exp\left(-\frac{\phi_b}{k_B T}\right)$$

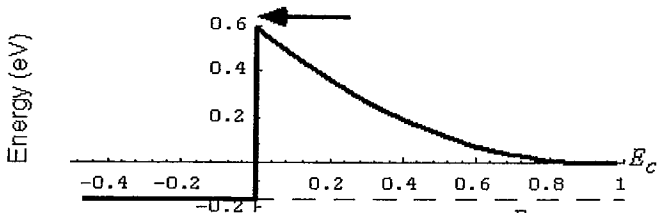
$$= \sqrt{\frac{1}{2\pi^3}} C \frac{m_n k_B^2 T^2}{\hbar^3} \exp\left(-\frac{\phi_b}{k_B T}\right) \tag{14}$$

where C is a numerical constant of the order of unity. With a proper choice of C, this equation coincides with eqs. (8) and (9).

Thermionic-field emission

In relatively highly doped semiconductors, the depletion region becomes so narrow that electrons can tunnel through the barrier near the top (see Fig. 4b). This process is called **thermionic-field emission**. In order to understand thermionic-field emission, we have to recall once again that the number of electrons with energies above a given energy E decreases exponentially with energy as exp[$-E/(k_BT)$]. On the other hand, the barrier transparency increases exponentially with the decrease in the barrier width. Hence, as the doping increases and the barrier becomes thinner, the dominant electron tunneling path occurs at lower energies than the top of the barrier (see Fig. 4b).

In degenerate semiconductors, especially in semiconductors with a small electron effective mass such as GaAs, electrons can tunnel through the barrier near or at the Fermi level, and the tunneling current is dominant. This mechanism is called **field emission** (see Fig. 4c).



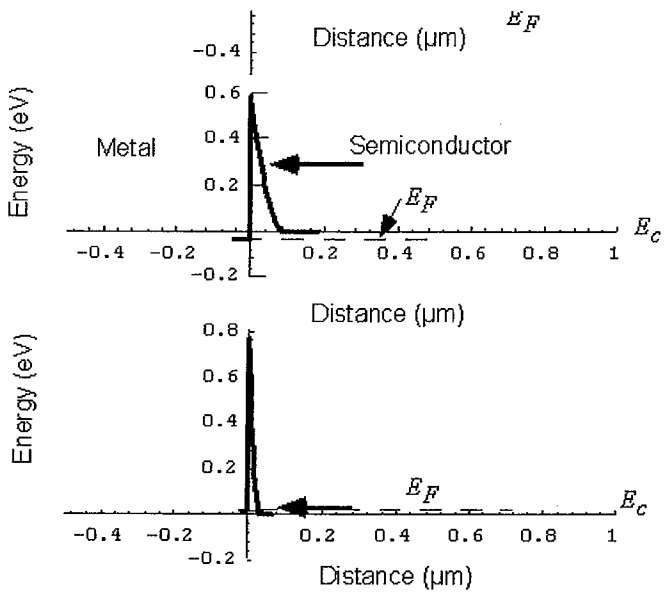


Fig. 4. Band diagrams of Schottky barrier junctions for GaAs for doping levels $N_d = 10^{15}$ cm^{-3} (top graph), $N_d = 10^{17}$ cm^{-3} (middle graph), and $N_d = 10^{18}$ cm^{-3} (bottom graph). Arrows indicate electron transfer across the barrier under forward bias. At very low doping levels, electrons go over the barrier closer to the top of the barrier (this process is called thermionic emission). At moderated doping levels, electrons tunnel across the barrier closer to the top of the barrier (this process is called thermionic-field emission). In highly doped degenerate semiconductors, electrons near the Fermi level tunnel across a very thin depletion region (this process is called field emission).

The current-voltage characteristic of a Schottky diode in the case of thermionic-field emission can be calculated using the same approach as for the thermionic model, except that in thermionic-field emission case, we have to evaluate the product of the tunneling transmission coefficient and the number of electrons at a given energy as a function of energy and integrate over the states in the conduction band. Such a calculation [see Rhoderick and Williams (1988)] yields the following expression for the current density in the thermionic-field emission regime under forward bias:

$$j = j_{stf} \exp\left(\frac{qV}{E_o}\right) \tag{15}$$

where

$$E_o = E_{oo} \coth\left(\frac{E_{oo}}{k_B T}\right) \tag{16}$$

$$E_{oo} = \frac{qh}{4\pi}\sqrt{\frac{N_d}{m_n \varepsilon_s}} = 1.85 \times 10^{-11}\left[\frac{N_d\left(\text{cm}^{-3}\right)}{\left(m_n / m_o\right)\left(\varepsilon_s / \varepsilon_o\right)}\right]^{1/2} \text{(eV)} \tag{17}$$

$$j_{stf} = \frac{A^* T \sqrt{\pi E_{oo}\left(\phi_b - qV - E_c + E_{Fn}\right)}}{k_B \cosh\left(E_{oo} / k_B T\right)} \exp\left[-\frac{E_c - E_{Fn}}{k_B T} - \frac{\left(\phi_b - E_c + E_{Fn}\right)}{E_o}\right] \tag{18}$$

In GaAs Schottky diodes, the thermionic-field emission becomes important for $N_d > 10^{17}$ cm^{-3} at 300 K and for $N_d > 10^{16}$ cm^{-3} at 77 K. In silicon, the corresponding values of N_d are several times larger. The forward j-V characteristics are shown in Fig. 5.

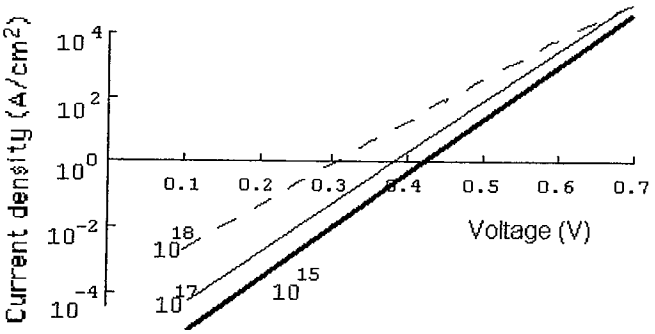


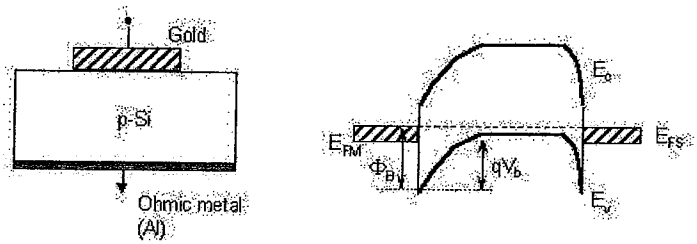
Fig. 5. Forward *j-V* characteristics of GaAs Schottky diodes doped at 10^{15}, 10^{17}, and 10^{18} cm^{-3} (curves are marked accordingly) at T = 300 K.

The resistance of the Schottky barrier in the field emission regime is quite low. Therefore metal-n^+ contacts are used as ohmic contacts. The specific contact resistance, r_c, decreases with the increase in the doping level of the semiconductor. (This resistance may vary from 10^{-3} Ωcm^2 to 10^{-7} Ωcm^2 or even smaller depending on semiconductor material, doping level, contact metal, and ohmic contact fabrication technology.)

A Schottky diode is a majority carrier device, where electron-hole recombination is usually not important. Hence, Schottky diodes have a much faster response under forward bias conditions than *p-n* junction diodes. Therefore, Schottky diodes are used in applications where the speed of a response is important, for example, in microwave **detectors**, **mixers**, and **varactors**.

Schottky Diode

- Structure of Schottky diode
  - Schottky contact/semiconductor/ohmic contact
  - What Schottky and ohmic metal systems do you apply for p-type Si?



Schottky Diode Electrostatics

- Built-in Voltage

$$V_0 = \left[\Phi_B - (E_c - E_{FN})_{BB}\right]/q$$

- Charge distribution

$$\rho = \begin{cases} qN_D & 0 \le x \le W \\ 0 & x \le W \end{cases}$$

- Electric field

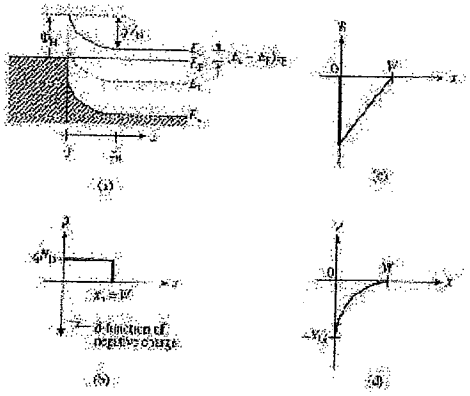
$$E(x) = -\frac{qN_D}{\varepsilon_s}(W - x)$$

- Potential

$$V(x) = -\frac{qN_D}{2\varepsilon_s}(W - x)^2$$

- Depletion width

$$W = \left[\frac{2\varepsilon_s}{qN_D}(V_0 - V_a)\right]^{1/2}$$



I-V Characteristics

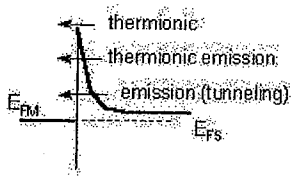
- Relatively low barrier for electrons in *n*-side
- Dominant current from the electron injection from *n*-side : *Thermonic emission* current
- At further forward bias, recombination and injection become important
- At reverse bias, electron injection from metal is dominant and carrier generation in the semiconductor depletion region is negligible
- Current density from S-to-M is known as the form of

$$J_{s\to M} = A^* T^2 \exp\left(-\frac{\Phi_B}{kT}\right)\exp\left(\frac{qV_a}{kT}\right)$$

where A^* = Richardson's constant

- Since $J_{S\to M} = J_{M\to S}$ at equilibrium (V_a=0)

$$J_{M\to S} = A^* T^2 \exp\left(-\frac{\Phi_B}{kT}\right)$$



- Therefore

$$J = J_S\left[\exp\left(\frac{qV_a}{kT}\right) - 1\right]$$

with $J_S = A^* T^2 \exp\left(-\frac{\Phi_B}{kT}\right)$

$A^* = 4\pi q m^* k^2/h^3$

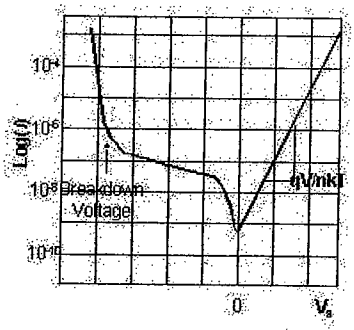
- m^*/m_0=0.66 or 2.2 for p- and n-type Si
- In general

$$J = J_S\left[\exp\left(\frac{qV_a}{nkT}\right) - 1\right]$$

with n=ideality factor

I-V Characteristics

- Important I-V characteristics are
  - Turn-on voltage
  - Ideality factor
  - Breakdown voltage
  - Series resistance



C-V Characteristics

- Depletion region only in semiconductor
- Capacitance

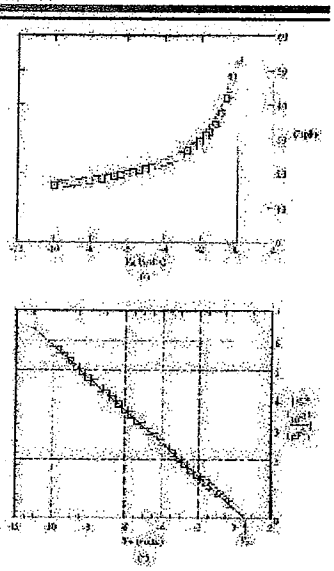
$$C = \varepsilon_s A / W$$

$$= \varepsilon_s A \left[\frac{2\varepsilon_s}{qN_D} (V_b - V_a) \right]^{1/2}$$

- For uniform doped semiconductor

$$\frac{1}{C^2} = \frac{2}{q N_D \varepsilon_s A^2} (V_b - V_a)$$

- This plot give out about the doping level and the built-in potential
- Combined with calculated Fermi energy, barrier height can be obtained



Prof. Dojin Kin site

OHMIC CONTACTS

In the case of a *p-n* diode, for example, contacts have to be provided to both *p*-type and *n*-type regions of the device in order to connect the diode to an external circuit. These contacts have to be as unobtrusive as possible, so that the current flowing through a semiconductor device and, hence, through the contacts, leads to the smallest parasitic voltage drop possible. Whatever voltage drop does occur across the contact has to be proportional to the current so that the contacts do not introduce uncontrollable and unexpected nonlinear elements into the circuit. Since

such contacts satisfy Ohm's law, they are usually called **ohmic contacts**.

As was discussed, a contact between a metal and a semiconductor is typically a Schottky barrier contact. However, if the semiconductor is very highly doped, the Schottky barrier depletion region becomes very thin, as illustrated in Fig. 4. At very high doping levels, a thin depletion layer becomes quite transparent for electron tunneling. This suggests that a practical way to make a good ohmic contact is to make a very highly doped semiconductor region between the contact metal and the semiconductor.

It may have been better to use a metal with a work function, F_m, which is equal to or smaller than the work function of a semiconductor, F_S. However, for most semiconductors, it is difficult to find such a metal acceptable for practical contacts.

Current-voltage characteristics of a Schottky barrier diode and of an ohmic contact are compared in Fig. 1. As was mentioned above, a good ohmic contact should have a linear current-voltage characteristic and a very small resistance that is negligible compared to the resistance of the active region of the semiconductor device. An ohmic contact with the *I-V* characteristic shown in Fig. 2 does not satisfy fully these conditions since the voltage drop across this contact is not negligibly small compared with the voltage drop across the Schottky diode at moderate current densities above 0.1 kA/cm^2.

As was discussed, the barrier between a metal and a semiconductor is usually smaller for semiconductors with smaller energy gaps.Hence, another way to decrease the contact resistance is to place a layer of a narrow gap highly doped semiconductor material between the active region of the device and the contact metal. Some of the best ohmic contacts to date have been made this way.

A quantitative measure of the contact quality is the **specific contact resistance**, r_c, which is the contact resistance of a unit area contact. Depending on the semiconductor material and on the contact quality, r_c can vary anywhere from 10^{-3} Ωcm^2 to 10^{-7} Ωcm^2 or even less.

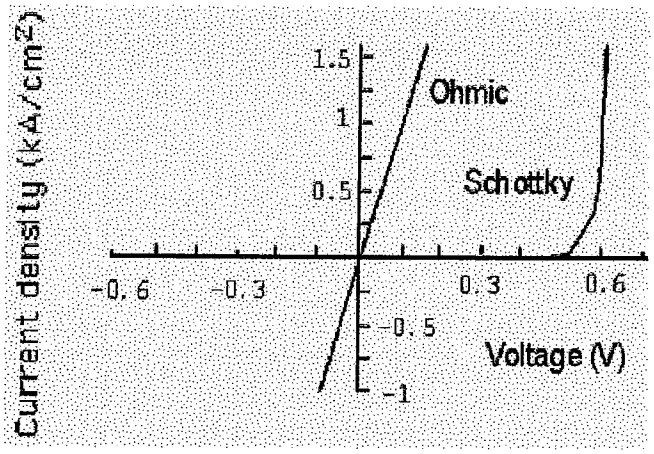


Fig. 1. Current-voltage characteristics of ohmic and Schottky barrier metal-semiconductor contacts to GaAs. (Schottky contact is to GaAs doped at 10^{15} cm^{-3}.) Ohmic contact resistance is 10^4 Ωcm^2.

Most semiconductor devices have either a sandwich structure or a planar structure, as illustrated in Fig. 2. The contact resistance of each contact in a sandwich structure contact is given by

$$R_c = \frac{\rho_c}{S}$$

(1)

A typical current density in a sandwich type device can be as high as 10^4 A/cm^2. Hence, the specific contact resistance of 10^{-5} Ωcm^2 would lead to a voltage drop on the order of 0.1 V. This may be barely acceptable. A larger specific contact resistance of 10^{-4} Ωcm^2 or so would definitely lead to problems, as we can see from Fig. 1.

These estimates show that a semiconductor material can become viable for applications in electronic devices only when good ohmic contacts with low contact resistances become available. Often, poor ohmic contacts become a major stumbling block for applications of new semiconductor materials.

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2. TMAH Etching Rates vs. Composition and Temperature

Similar to KOH, the TMAH etch rate varies exponentially with temperature. Table 4 relates **silicon** orientation-dependent etch rates of TMAH to percent composition, temperature, and orientation. Table 4 is taken directly from [2].

Etchant	Temperature (°C)	Direction (plane)	Etch rate (μm min^{-1})	Remarks Resources
5% TMAH: 95% H_2O	60	(100)	0.33	[7]
	70		0.48	
	80		0.87	
	90		1.4	
	60	(110)	0.64	
	70		0.74	
	80		1.4	
	90		1.8	
	60	(111)	0.026	
	90		0.034	
10% TMAH: 90% H_2O	60	(100) 0.28		[7]
	70		0.41	
	80		0.72	
	90		1.2	
2% TMAH:	80 (100)		0.65	[8]

98% H_2O		(111)	0.41		
5% TMAH:	80 (100)		0.63	[8]	
95% H_2O		(111)	0.013		
10% TMAH:	80 (100)		0.57	[8]	
90% H_2O		(111)	0.014		
22% TMAH in H_2O	90 (100)		0.9	(110) is fastest without surfactant	[9]
		(110)	1.8		
		(111)	0.018		
22% TMAH in H_2O + 0.5% surfactant	90 (100)		0.6	(100) is fastest with surfactant	[9]
		(110)	0.12		
		(111)	0.01		
22% TMAH in H_2O + 1% surfactant	90 (100)		0.6	Surfactants effect saturates	[9]
		(110)	0.1		
		(111)	0.009		

\

E EDP

Similar to KOH, EDP is often used for fast removal and **silicon** micromachining. Table 5 relates **silicon** orientation-dependent etch rates in EDP solutions to Temperature and Orientation.

Etchant	Temperature (°C)	Direction (plane)	Etch rate (μm min^{-1})	Remarks	Reference
500 ml $NH_2(CH_2)_2NH_2$: 88g $C_6H_4(OH)_2$: 234 ml H_2O	110 (100)		0.47	EDP 'T' etch	[10]
		(110)	0.28	Oldest EDP formula	
		(111)	0.028	ER rises to > 0.83 μm/min after exposure to	

				oxygen	
500 ml $NH_2(CH_2)_2NH_2$: 160g $C_6H_4(OH)_2$: 160 ml H_20	115	(100)	0.45	EDP 'F' etch Fast etch rate Must be used at high T to avoid residue	[11]
F etch above w/1.0g $C_6H_4N_2$	115 (100)			Faster w/ pyrazine Less sensitive to oxygen Smoother	[11]
F etch above w/3.0g $C_6H_4N_2$	115 (100)		1.35		[11]
500 ml	50	(100)	0.075	EDP 'S' etch	[11]
$NH_2(CH_2)_2NH_2$:	75	(100)	0.22	Slower etch rate	
80g $C_6H_4(OH)_2$:	95	(100)	0.43	Suitable for	
3.6 $C_6H_4N_2$: 66ml	105	(100)	0.57	lower	
H_20	110	(100)	0.75	temperature use without residue	
46.4 mol% $NH_2(CH_2)_2NH_2$: 4 mol% $C_6H_4(OH)_2$: 49.4 mol% H_20	118 (100)	(110) (111)		Stops on p^{++}	[12]
250 ml $NH_2(CH_2)_2NH_2$: 45g $C_6H_4(OH)_2$: 120ml H_20	110 (100)	(111)			[13]

F Isotropic Silicon Etches

Often, isotropic etchants having dissolution rates independant of orientation are needed. These chemical mixtures tend to uniformly remove material, and are limited by the mass transport of chemical species to the crystal surface. The actual surface reaction rates are so great that variations to atomic structure do not alter the reaction speed relative to chemical transport.

Table 6 lists several common recipes and is taken directly from [14].

Formula	Comments	Reference
HF, HNO_3		See [14] p73

HF, HNO_3, H_20 or CH_3COOH	Various combinations give different etch rates	[15]
900ml HNO_3, 95 ml HF, 5ml CH_3COOH, 14g $NaClO_2$	15 μm/min	[16]
745 ml HNO_3, 105 ml HF, 75 ml CH_3COOH, 75 ml $HClO_4$	170 A/sec	[17]
50 ml HF, 50 ml CH_3COOH, 200 mg $KMnO_4$(fresh)	Epi Etching 0.2 μm/min	[18]
108 ml HF, 350g NH_4F per L H_20	Epi Etching n type 0.2-0.6 ohm-cm; 0.43 A/min p type 0.4 ohm-cm; 0.45 A/min p type 15 ohm-cm; 0.23 A/min	[19]

G Silicon Defect Delineation Etches

Certain chemical etchants are strongly dependent on defects, and defect structures in the single crystal **silicon**. These etchants are commonly used to high-light or delineate defects in the material.

Table 7 lists the most common defect delineation mixtures, and is taken directly from [14]

Formula		Name	Application Shelf Life	Ref
1	1 ml HF, 1 ml C_2O_3(5M)	Sirtl	111 **Silicon** Approx 5min etch	5 min [20]
2	1 ml HF, 3 ml HNO_3, 1 ml CH_3COOH	Dash	111 oe 100 n or p (works best on p) Approx 15 hr etch	8 h [21]
3	2 ml HF, 1 ml $K2Cr_2O_7$ (0.15M)	Secco	100 or 111 **silicon**	5 min [21]
	2 ml HF, 1 ml Cr_2O_3 (0.15M)	Secco	100 or 111 **silicon**	5 min [21][20]
4	200 ml HF, 1 HNO_3		P-N delineation	[20]
5	60 ml HF, 30 ml HNO_3 60 ml H_20 60 ml CH_3COOH, 30 ml (1g CrO_3 to 2 ml H_20)	Jenkins Wright	general use does not roughen defect free regions Approx 30 min etch	6 wks [21][20] [22]
6	2 ml HF, 1 ml HNO_3, 2 ml $AgNO_3$(0.65M in	Silver epitaxial	layer faults	[20]

	H20)			
7	5 gm H_5IO_6, 5 mg Kl in 50 ml H_2O, 2 ml HF	Sponheimer Mills	Etch 5-20 seconds junction delineation	[22]

8 Shipley	112°			[23]
9	6 ml HF, 19 ml HNO			[23]
10	(150g/l (1.5M) CrO_3 to H_20) to HF 1:1	Yang		[24]
11	600 ml HF, 300 ml HNO_3 28g $Cu(NO_3)_2$, 3 ml H_20	Copper Etch		[25]
12	1000 ml H_2O, 1 drop (1.0N) KOH 3.54g kBr, .708g $KbrO_3$			[25]
13 55g	$CuSO_4$, SH20, 950 ml H_20, 50 ml Hf	Copper Displacement		[25]
14	1 ml HF, 3 ml HNO_3	White	15 secs. PN Junction etch with stron light	
15	3 ml HF, 5 ml HNO_3, 3 ml CH_3COOH	CP-4	10 sec – 3 min P-N Junctions	[26]
16a	25 ml HF, 18 ml HNO_3, 5 ml CH_3COOH/.1Br2 10 ml H_20, 1g $Cu(NO_3)_2$	SD1	2-4 min reveals edge and mixed dislocations	[26]
16b	100 ml HF; .1 to .5 ml HNO3		P stain	[26]
16c	50 ml dilute $Cu(NO_3)_2$ 1 to 2 drops HF		N stain	[26]
16d	4% NaOH add 40 NaClO until no H_2 evolution from Si		80°C specimen thinning (float specimen on	[26]

			surface of etch)	
17	300 ml HNO_3, 600 ml HF 2 ml Br_2, 24g $Cu(NO_3)_2$ dilute 10:1 wtih H_2O	Sailer	Etch 4 hr Epi Stacking Faults	[27]
18	a) 1) 75g CrO_3 in 1000 ml H_2O mix 1 part 1) to 2 parts 48% HF	Schimmel	Resistivity greater than .2 ohm-cm (111) oe (100) approx 5 min	
	b) mix part 1) to 2 parts 48% HF to 1.5 parts H_2O		Resistivity less than .2 ohm-cm	
19 5g	H_5IO_6, 50 ml H_2O, 2 ml HF, 5mg KI	Periodic HF	Junction Deliniation	

H Conclusion

There are many wet-chemical etch recipes known for etching **silicon**. These processes are used for a variety of applications including micromachining, **cleaning**, and defect delineation. The detailed behaviour and rate of the etchant will vary between laboratory enviroments and exact processes. However, the data and phenomena recorded above have been reported by many researchers and manufactures.
For further details the reader is encourage to fully explore the direct and indirect references sited.

I References

[1] K. Sato et al.[Characterization of orientation-dependent ethcing properties of single-crystal **silicon**: effects of KOH concetration (*Sensors and Actuators A 64* (1988) 87-93)]

[2] R. Hull [*Properties of Crystalline **Silicon*** (INSPEC, London, 1999)]

[3] H. Seidel, L. Cseprege, A. Heuberger, H. Baumgarel [*J. Electrochem. Soc. (USA)* vol. 137 (1990) p. 3626-32]

[4] D.L. Kendall [*Annu. Rev. Mater. Sci (USA)* vol.9 (1979) p.373]

[5] J.B. Price [*Semiconductor **Silicon** –1973* Eds. H.R. Huff, R.R. Burgess (E;

[6] M. Shikida, K. Sato, K. Tokoro, D. Uchikawa [Dept. of Micro Sysytems

Etchant	Temperature (°C)	Direction (plane)	Etch rate (μm min^{-1})	Remarks	Reference
20% KOH: 80% H_2O	20	(100)	0.025	Near Peak etch rate at the conc. across temperature	[3]
	40	(100)	0.188		
	60	(100)	0.45		
	80	(100)	1.4		
	100	(100)	4.1		
30% KOH: 70% H_2O	20	(100)	0.024	Smoother surfaces than at lower concentration	[3]
	40	(100)	0.108		
	60	(100)	0.41		
	80	(100)	1.3		
	100	(100)	3.8		
	20	(110)	0.035		
	40	(110)	0.16		
	60	(110)	0.62		
	80	(110)	2.0		
	100	(110)	5.8	Faster etch rate for (110) than for (100)	
40% KOH: 60% H_2O	20	(100)	0.020	[3]	
	40	(100)	0.088		
	60	(100)	0.33		
	80	(100)	1.1		
	100	(100)	3.1		
20% KOH: 80% 4 H_2O: 1 IPA)	20	(100)	0.015	Lower etch rate	[3]
	40	(100)	0.071	Smoother	
	60	(100)	0.28	Less undercutting	
	80	(100)	0.96	Lower (100) : (111) etch-rate ration	
	100	(100)	2.9		
44% KOH: 56% H_2O	120 (100)		5.8	High Temperature	[4]
		(110)	11.7		
		(111)	0.02		

23.4% KOH: 63.3% H_2O: 13.3% IPA	80 (100)	(110)	1.0 0.06	Sensitive to boron concentration	[5]

D Anisotropic TMAH (tetramethylammonium hydroxide) Etching

Similar to KOH etching, TMAH is commonly used for fast removal and **silicon** micromachining.

1. TMAH Etching Rates vs. Orientation

The orientation dependence of the TMAH etch rate is similar to KOH and varies similarly in accordance to the atomic organization of the crystallographic plane. Table 3 relates **silicon** orientation-dependent etch rates of TMAH (20.0wt%, 79.8°C) to orientation. Table 3 is taken directly from [6].

Orientation	Etching rate (μm min^{-1})	Etching rate ratio (i j k)/(100)	(i j k)/(111)
100	0.603	1.000	37
110	1.114	1.847	68
210	1.154	1.914	70
211	1.132	1.877	69
221	1.142	1.894	69
310	1.184	1.964	72
311	1.223	2.028	74
320	1.211	2.008	73
331	1.099	1.823	67
530	1.097	1.819	66
540	1.135	1.882	69
111	0.017	0.027	1

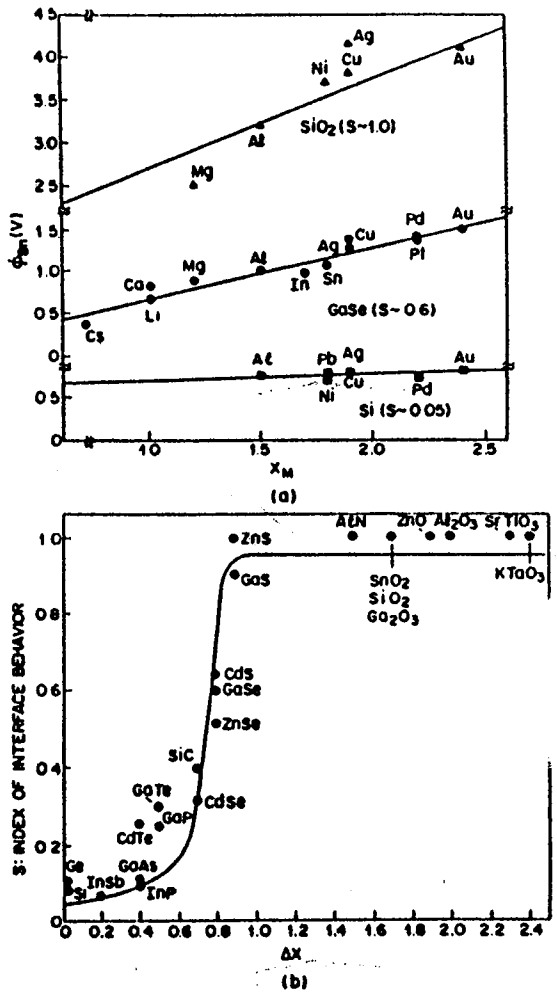

Fig. 20 (a) Barrier height versus electronegativity of metals deposited on Si, GaSe, and SiO_2. (b) Index of interface behavior S as a function of the electronegativity difference of the semiconductors. (After Kurtin, McGill, and Mead, Ref. 29.)

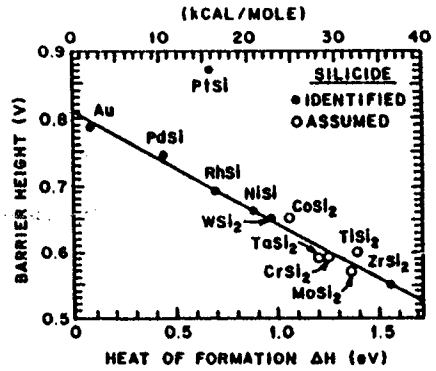

Fig. 21 Barrier height of transition metal silicides versus heat of formation. (After Andrews, Ref. 71.)

binding energy of silicon (4.67 eV). This value is very close to the value ΔH obtained from Eq. 78 by setting $\phi_{Bn} = 0$.

5.5.2 Measurement of Barrier Height

Basically, four methods are used to measure the barrier height of a metal–semiconductor contact: the current–voltage, activation energy, capacitance–voltage, and photoelectric methods.[30]

Current–Voltage Measurement For moderately doped semiconductors, the I–V characteristics in the forward direction with $V > 3kT/q$ is given by Eq. 49:

$$J = A^{**}T^2 \exp\left(-\frac{q\phi_{B0}}{kT}\right) \exp\left[\frac{q(\Delta\phi + V)}{kT}\right] \tag{79}$$

where ϕ_{B0} is the zero-field asymptotic barrier height as shown in Fig. 15, A^{**} is the effective Richardson constant, and $\Delta\phi$ is the Schottky barrier lowering. Since both A^{**} and $\Delta\phi$ are functions of the applied voltage, the forward J–V characteristic (for $V > 3kT/q$) is represented by $J \sim \exp(qV/nkT)$, as given previously in Eq. 53, where n is the ideality factor:

$$n = \frac{q}{kT}\frac{\partial V}{\partial(\ln J)}$$

$$= \left[1 + \frac{\partial \Delta\phi}{\partial V} + \frac{kT}{q}\frac{\partial(\ln A^{**})}{\partial V}\right]^{-1}. \tag{80}$$

Typical examples are shown in Fig. 22, where $n = 1.02$ for the W–Si diode and $n = 1.04$ for the W–GaAs diode.[31] The extrapolated value of current

1eV = 10,000°K

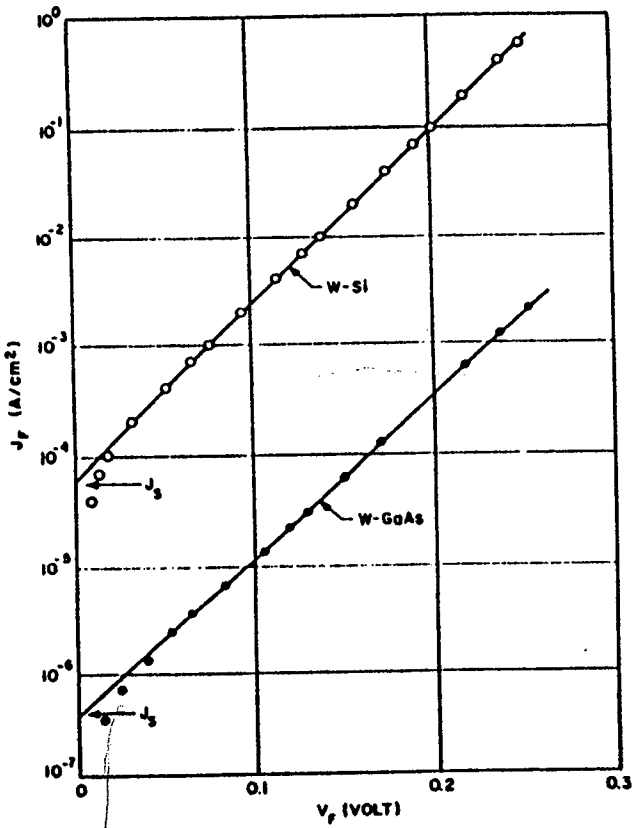

Fig. 22 Forward current density versus applied voltage of W-Si and W-GaAs diodes. (After Crowell, Sarace, and Sze, Ref. 31.)

density at zero voltage is the saturation current J_S, and the barrier height can be obtained from the equation

$$\phi_{Bn} = \frac{kT}{q} \ln\left(\frac{A^{**}T^2}{J_S}\right). \tag{81}$$

The value of ϕ_{Bn} is not very sensitive to the choice of A^{**}, since at room temperature, a 100% increase in A^{**} will cause an increase of only 0.018 V in ϕ_{Bn}. The theoretical relationship between J_S and ϕ_{Bn} (or ϕ_{Bp}) at room temperature is plotted in Fig. 23 for $A^{**} = 120$ A/cm²/K². For other values of A^{**}, parallel lines can be drawn on this plot to obtain the proper

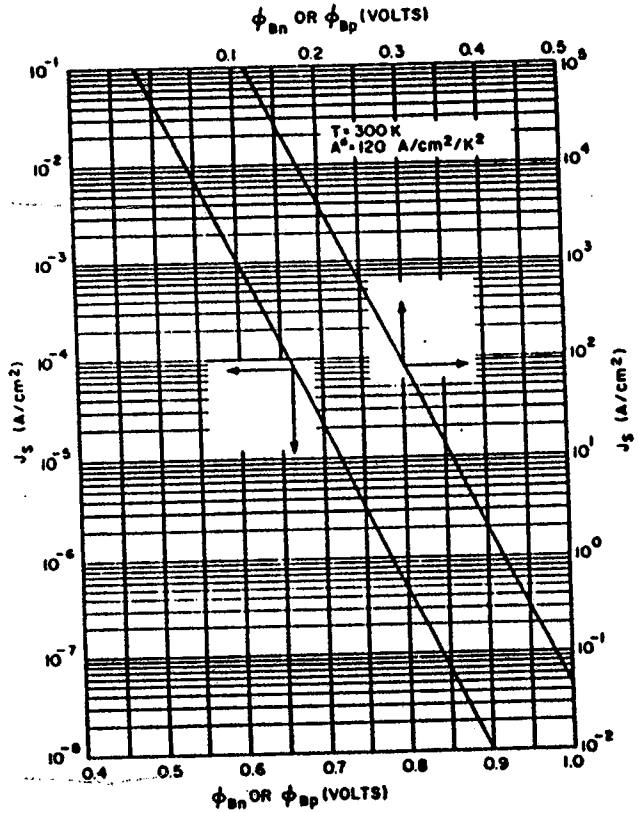

Fig. 23 Theoretical saturation current density at 300 K versus barrier height for a Richardson constant of 120 A/cm²/K².

relationship. In the reverse direction, the dominant effect is due to the Schottky-barrier lowering, or

$$J_R \simeq J_S \quad (\text{for } V_R > 3kT/q)$$
$$= A^{**}T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \exp\left(+\frac{q\sqrt{q\mathcal{E}/4\pi\epsilon_s}}{kT}\right) \tag{82}$$

where

$$\mathcal{E} = \sqrt{\frac{2qN_D}{\epsilon_s}\left(V + V_{bi} - \frac{kT}{q}\right)}.$$

If the barrier height $q\phi_{Bn}$ is sufficiently smaller than the bandgap so that the

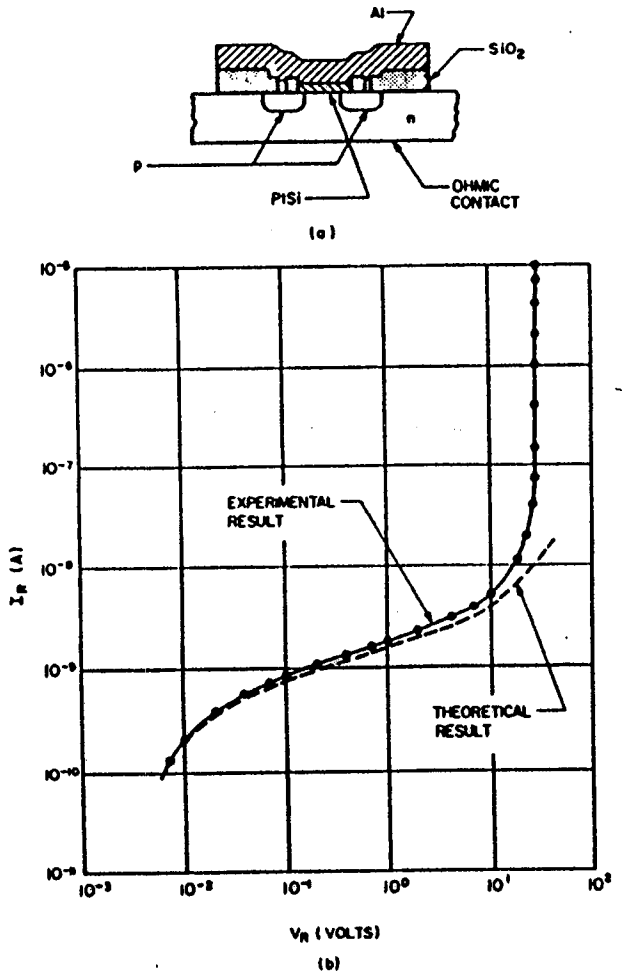

Fig. 24 (a) PtSi–Si diode with a diffused guard ring. (b) Comparison of experimental with theoretical prediction of Eq. 82 for a PtSi–Si diode. (After Lepselter and Sze, Ref. 32.)

depletion-layer generation–recombination current is small in comparison with the Schottky emission current, then the reverse current will increase gradually with the reverse bias as given by Eq. 82.

For most of the practical Schottky diodes, however, the dominant reverse current component is the edge-leakage current, which is caused by

the sharp edge around the periphery of the metal plate. This sharp-edge effect is similar to the junction curvature effect (with $r_j \to 0$) as discussed in Chapter 2. To eliminate this effect, metal–semiconductor diodes have been fabricated with a diffused guard ring as shown[32] in Fig. 24*a*. The guard ring is a deep p-type diffusion, and the doping profile is tailored to give the p-n junction a higher breakdown voltage than that of the metal–semiconductor contact. Because of the elimination of the sharp-edge effect, near-ideal forward and reverse I–V characteristics have been obtained. Figure 24*b* shows a comparison between experimental measurement from a PtSi–Si diode with guard ring and theoretical calculation based on Eq. 82. The agreement is excellent. The sharp increase of current near 30 V is due to avalanche breakdown and is expected for the diode with a donor concentration of 2.5×10^{16} cm^{-3}.

The efficacy of guard ring structures in preventing premature breakdown and surface leakage can be ascertained by studying reverse leakage current as a function of diode diameter at constant reverse bias. For this purpose, arrays of Schottky diodes with different diameters can be formed on the semiconductor. Figure 25 shows the measured reverse leakage currents as

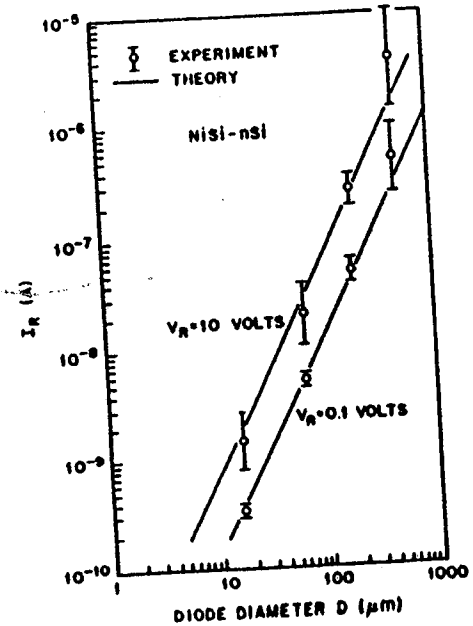

Fig. 25 Reverse leakage current as a function of diode diameter for NiSi–Si diodes formed on n-type silicon with $N_D = 6 \times 10^{15}$ cm^{-3}. (After Andrews and Koch, Ref. 33.)

activation energy plots of the forward current in Al–n-type Si contacts annealed at various temperatures.[47] The slopes of these plots indicate a nearly linear increase of effective Schottky barrier height from 0.71 to 0.81 V for annealing temperatures between 450 and 650°C. These observations were also confirmed with I–V and C–V measurements.

Obviously, when the Al–Si eutectic temperature (~580°) is reached, the true metallurgical nature of the metal–semiconductor must be considerably modified. Determination of the ordinate intercepts from the plots shown in Fig. 27 indicates that the electrically active area increases by a factor of 2 when the annealing temperature exceeds the Al–Si eutectic temperature.

Capacitance–Voltage Measurement The barrier height can also be determined by the capacitance measurement. When a small ac voltage is superimposed upon a dc bias, charges of one sign are induced on the metal surface and charges of the opposite sign in the semiconductor. The relationship between C and V is given by Eq. 9. Figure 28 shows some typical results where $1/C^2$ is plotted against the applied voltage. From the

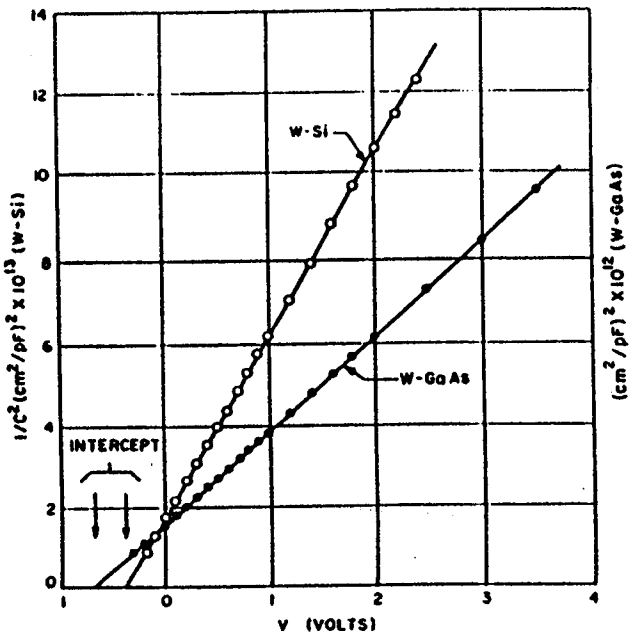

Fig. 28 $1/C^2$ versus applied voltage for W-Si and W-GaAs diodes. (After Crowell, Sarace, and Sze, Ref. 31.)

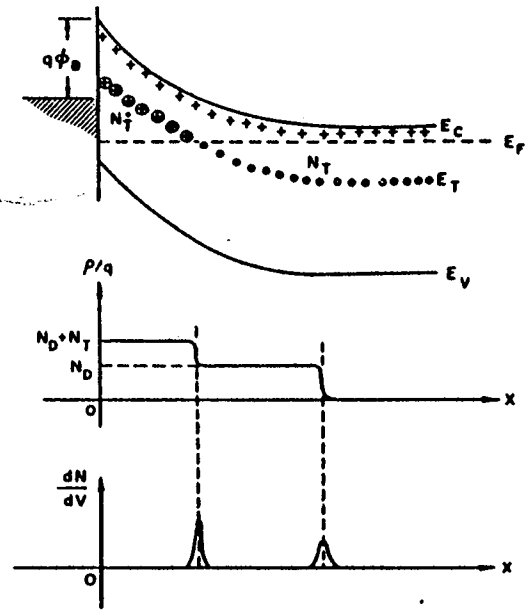

Fig. 29 Semiconductor with one shallow donor level and one deep donor level. N_D and N_T are the shallow donor and deep donor concentration, respectively. (After Roberts and Crowell, Ref. 35.)

intercept on the voltage axis, the barrier height can be determined:[31,34]

$$\phi_{Bn} = V_i + V_n + \frac{kT}{q} - \Delta\phi \tag{85}$$

where V_i is the voltage intercept, and V_n the depth of the Fermi level below the conduction band, which can be computed if the doping concentration is known. From the slope the carrier density can be determined (Eq. 10c). (This method can also be used to measure the doping variation in an epitaxial layer.)

The C–V measurement can also be used to study deep impurity levels. Figure 29 shows a semiconductor with one shallow doping level and one deep donor level.[35] Under bias, all the donors above the Fermi level will be ionized, giving a higher doping concentration near the interface. When a small ac signal is superimposed on the dc bias and when the deep level can follow the signal, there will be an additional contribution of dN/dV to the capacitance. Figure 30 shows $1/C^2$ versus V for various frequencies. The low-frequency curves can reveal the properties of the deep impurities. To obtain the barrier height of semiconductor with one shallow level and one

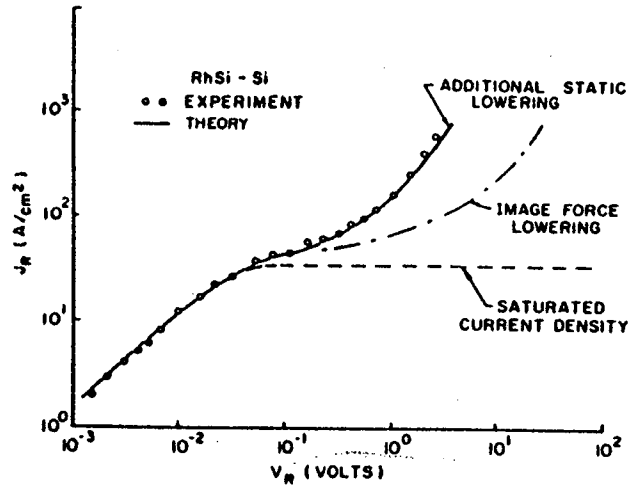

Fig. 26 Theory and experiment of reverse characteristics for a RhSi–Si diode. (After Andrews and Lepselter, Ref. 19.)

a function of diode diameter.[33] The solid lines drawn through the experimental data have slopes equal to 2, showing that the leakage currents are proportional to the device area. If, on the other hand, the leakage currents are dominated by edge effects, the data would be expected to lie along straight lines with slopes equal to unity.

For some Schottky diodes, the reverse current has an additional voltage dependence. This dependence arises from the fact that if the metal–semiconductor interface is free from intervening layers of oxide and other contaminants, the electrons in the metal have wave functions that penetrate into the semiconductor energy gap. This is a quantum-mechanical effect that results in a static dipole layer at the metal–semiconductor interface. The dipole layer causes the intrinsic barrier height to vary slightly with the field, so $\partial\phi_{Bn}/\partial\mathscr{E}_m \neq 0$. To a first approximation the static lowering can be expressed as

$$(\Delta\phi)_{static} \simeq \alpha'\mathscr{E}_m \tag{83}$$

where $\alpha \simeq \partial\phi_{Bn}/\partial\mathscr{E}_m$. Figure 26 shows good agreement between the theory and measurements of the reverse current in a RhSi–Si diode, based on an empirical value of $\alpha \simeq 17$ Å.

Activation Energy Measurement The principal advantage of Schottky-barrier determination by means of an activation energy measurement is that no assumption of electrically active area is required. This feature is particularly important in the investigation of novel or

unusual metal–semiconductor interfaces, because often the true value of the contacting area is not known. In the case of poorly cleaned or incompletely reacted surfaces, the electrically active area may be only a small fraction of the geometric area. On the other hand, a strong metallurgical reaction could result in rough nonplanar metal–semiconductor interface with an electrically active area that is larger than the apparent geometric area.

If Eq. 49 is multiplied by A_e, the electrically active area, we obtain

$$\ln(I_F/T^2) = \ln(A_e A^{**}) - q(\phi_{Bn} - V_F)/kT \tag{84}$$

where $q(\phi_{Bn} - V_F)$ is the activation energy. Over a limited range of temperature (e.g., 273 K < T < 373 K), the value of A^{**} and ϕ_{Bn} are essentially temperature-independent. Thus for a given forward bias V_F, the slope of a plot of $\ln(I_F/T^2)$ versus $1/T$ yields the barrier height ϕ_{Bn}, and the ordinate intercept at $1/T = 0$ yields the product of the electrically active area A_e and the effective Richardson constant A^{**}.

To illustrate the importance of the activation energy method in the investigation of interfacial metallurgical reactions, Figure 27 shows the

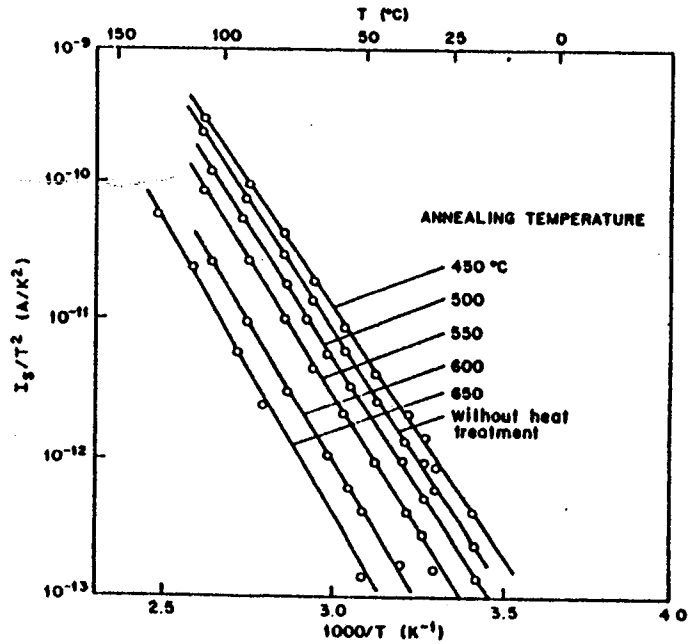

Fig. 27 Activation energy plots for determination of barrier height. (After Chino, Ref. 47.)

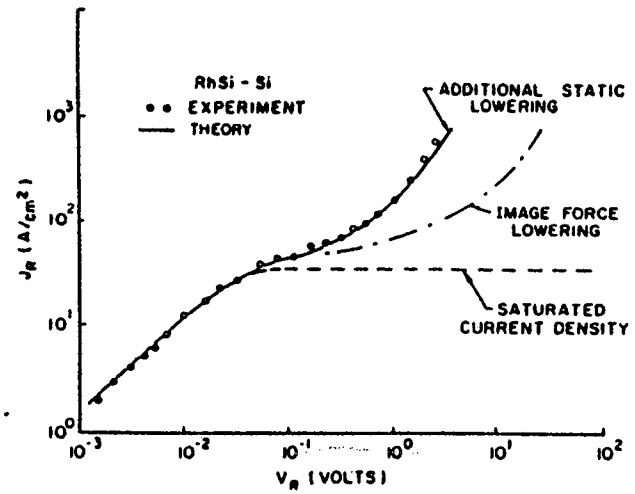

Fig. 26 Theory and experiment of reverse characteristics for a RhSi–Si diode. (After Andrews and Lepselter, Ref. 19.)

a function of diode diameter.[19] The solid lines drawn through the experimental data have slopes equal to 2, showing that the leakage currents are proportional to the device area. If, on the other hand, the leakage currents are dominated by edge effects, the data would be expected to lie along straight lines with slopes equal to unity.

For some Schottky diodes, the reverse current has an additional voltage dependence. This dependence arises from the fact that if the metal–semiconductor interface is free from intervening layers of oxide and other contaminants, the electrons in the metal have wave functions that penetrate into the semiconductor energy gap. This is a quantum-mechanical effect that results in a static dipole layer at the metal–semiconductor interface. The dipole layer causes the intrinsic barrier height to vary slightly with the field, so $\partial\phi_{Bn}/\partial\mathscr{E}_m \neq 0$. To a first approximation the static lowering can be expressed as

$$(\Delta\phi)_{static} \simeq \alpha\mathscr{E}_m \tag{83}$$

where $\alpha \simeq \partial\phi_{Bn}/\partial\mathscr{E}_m$. Figure 26 shows good agreement between the theory and measurements of the reverse current in a RhSi–Si diode, based on an empirical value of $\alpha \simeq 17$ Å.

Activation Energy Measurement The principal advantage of Schottky-barrier determination by means of an activation energy measurement is that no assumption of electrically active area is required. This feature is particularly important in the investigation of novel or unusual metal–semiconductor interfaces, because often the true value of the contacting area is not known. In the case of poorly cleaned or incompletely reacted surfaces, the electrically active area may be only a small fraction of the geometric area. On the other hand, a strong metallurgical reaction could result in rough nonplanar metal–semiconductor interface with an electrically active area that is larger than the apparent geometric area.

If Eq. 49 is multiplied by A_r, the electrically active area, we obtain

$$\ln(I_F/T^2) = \ln(A_r A^{**}) - q(\phi_{Bn} - V_F)/kT \tag{84}$$

where $q(\phi_{Bn} - V_F)$ is the activation energy. Over a limited range of temperature (e.g., 273 K $< T <$ 373 K), the value of A^{**} and ϕ_{Bn} are essentially temperature-independent. Thus for a given forward bias V_F, the slope of a plot of $\ln(I_F/T^2)$ versus $1/T$ yields the barrier height ϕ_{Bn}, and the ordinate intercept at $1/T = 0$ yields the product of the electrically active area A_r and the effective Richardson constant A^{**}.

To illustrate the importance of the activation energy method in the investigation of interfacial metallurgical reactions, Figure 27 shows the

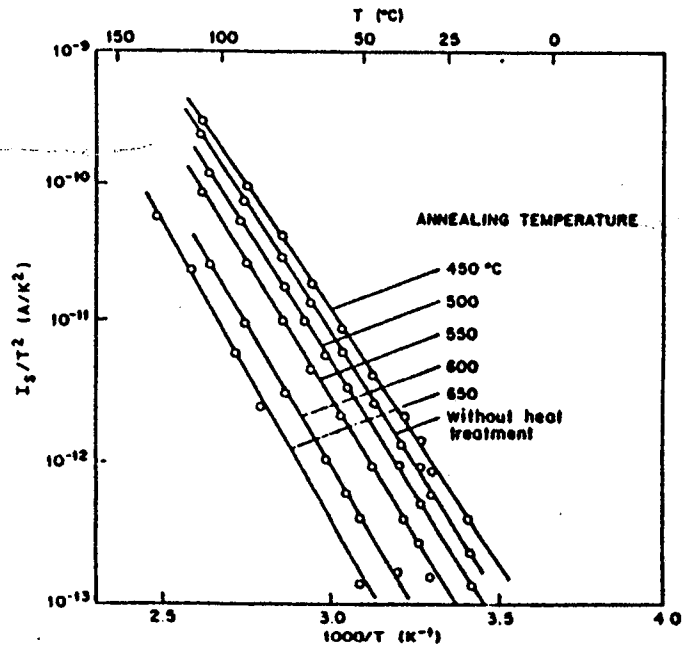

Fig. 27 Activation energy plots for determination of barrier height. (After Chino, Ref. 47.)

or

$$\sqrt{R} \sim h(\nu - \nu_0). \tag{86b}$$

When the square root of the photoresponse is plotted as a function of photon energy, a straight line should be obtained, and the extrapolated value on the energy axis should give directly the barrier height. Figure 32 shows the photoresponse of W–Si and W–GaAs diodes, the barrier heights of 0.65 and 0.80 eV, respectively.

The photoelectric measurement can be used to study other device and material parameters. It has been used to determine the image-force dielectric constant of Au–Si diodes.[10] By measuring the shift of the photothreshold under different reverse biases, one can determine the image-force lowering $\Delta\phi$. From a plot of $\Delta\phi$ versus $\sqrt{\mathscr{E}}$, the image for dielectric constant (ϵ_i/ϵ_0) can be determined, as shown previously in Fig. 5. The photoelectric measurement has been used to study the temperature dependence of the barrier height.[38] The photothreshold is measured as a function of temperature of Au–Si diodes. The shift of photothreshold correlates reasonably well with the temperature dependence of the silicon-bandgap. This result implies that the Fermi level at the Au–Si interface is

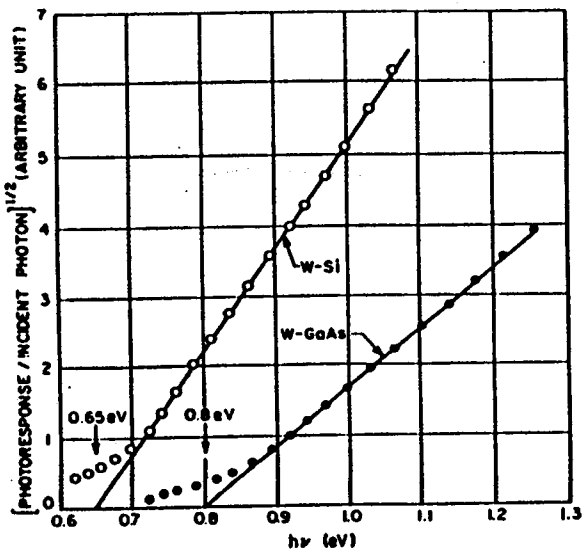

Fig. 32 Square root of the photoresponse per incident photon versus photon energy for W–Si and W–GaAs diodes. The extrapolated values are the corresponding barrier height $q\phi_{Bn}$. (After Crowell, Sarace, and Sze, Ref. 31.)

Table 3 Measured Schottky-Barrier Heights (Volts at 300 K)

Semiconductor	Type	E_g (eV)	As	Al	Au	Cr	Cu	Hf	In	Mg	Mo	Ni	Pb	Pd	Pt	Ta	Ti	W
Diamond	p	5.47			1.71				0.64			0.49	0.38					0.48
Ge	n	0.66	0.54	0.48	0.59		0.52		0.55								0.50	0.67
Ge	p		0.50		0.30					0.40	0.68	0.61		0.81	0.90		0.61	0.45
Si	n	1.12	0.78	0.72	0.80	0.61	0.58	0.58			0.42	0.51	0.55					
Si	p		0.54	0.58	0.34	0.50	0.46									1.00		
SiC	n	3.00		2.00	1.95													
AlAs	n	2.16			1.20													
AlSb	p	1.63			0.55													
BN	p	7.50			3.10													
BP	p	6.00			0.87										0.84	0.85		0.80
GaSb	n	0.67			0.60													
GaAs	n	1.42	0.88	0.80	0.90		0.82	0.72										
GaAs	p		0.63		0.42			0.68							1.45		1.12	
GaP	n	2.24	1.20	1.07	1.30	1.06	1.20	1.84		1.04	1.13	1.27						
GaP	p				0.72													
InSb	n	0.16	0.18*		0.17*													
InAs	p	0.33			0.47*													
InP	n	1.29	0.54		0.52													
InP	p				0.76								0.45	0.59	0.62	1.10	0.84	
CdS	n	2.43	0.56	Ohmic	0.78		0.50									0.37		
CdSe	n	1.70	0.43		0.49		0.33									0.76		
CdTe	n		0.81	0.76	0.71										0.68	0.75	0.30	
ZnO	n	3.20		0.68	0.65		0.45			0.30					1.87	1.84	1.10	
ZnS	n	3.60	1.65	0.80	2.00		1.75			1.50	0.82			1.16		1.40		
ZnSe	n		1.21	0.76	1.36		1.10			0.91			0.96	0.95				
PbO	n		0.95							0.93								

Table 4 Barrier Height of Metal Silicide on *n*-Type Si

Metal Silicide	ϕ_{Bn} (V)	Structure	Forming Temperature (°C)	Melting Temperature (°C)
CoSi	0.68	Cubic	400	1460
$CoSi_2$	0.64	Cubic	450	1326
$CrSi_2$	0.57	Hexagonal	450	1475
HfSi	0.53	Orthorhombic	550	2200
IrSi	0.93	—	300	—
MnSi	0.76	Cubic	400	1275
$Mn_{11}Si_{19}$	0.72	Tetragonal	800*	1145
$MoSi_2$	0.55	Tetragonal	1000*	1980
Ni_2Si	0.7–0.75	Orthorhombic	200	1318
NiSi	0.66–0.75	Orthorhombic	400	992
$NiSi_2$	0.7	Cubic	800*	993
Pd_2Si	0.72–0.75	Hexagonal	200	1330
PtSi	0.84	Orthorhombic	300	1229
RhSi	0.69	Cubic	300	—
$TaSi_2$	0.59	Hexagonal	750*	2200
$TiSi_2$	0.60	Orthorhombic	650	1540
WSi_2	0.65	Tetragonal	650	2150
$ZrSi_2$	0.55	Orthorhombic	600	1520

*Can be ≤ 700°C under clean interface condition.

pinned in relation to the valence-band edge, and this is in agreement with our discussion in Section 5.5.1.

Measured Barrier Heights. The *I–V*, *C–V*, activation energy, and photoelectric methods have been used to measure the barrier heights. For intimate contacts with clean interface, these methods generally yield consistent barrier heights within ±0.02 V. A large discrepancy between different methods may result from such causes as contamination in the interface, intervening insulating layer, edge leakage current, or deep impurity levels.

The measured Schottky barrier heights are listed[39–41] in Table 3 for some elemental and compound semiconductors. The barrier heights are representative values for metal–semiconductor contacts made by deposition of high-purity metals in a good vacuum system onto cleaved or chemically cleaned semiconductor surfaces. As expected, silicon and GaAs metal–semiconductor contacts are most extensively studied. Among the metals, gold, aluminum, and platinum are most commonly used. The barrier heights of metal silicides on *n*-type silicon are listed[42–43a] in Table 4.

It should be pointed out that the barrier height is generally sensitive to

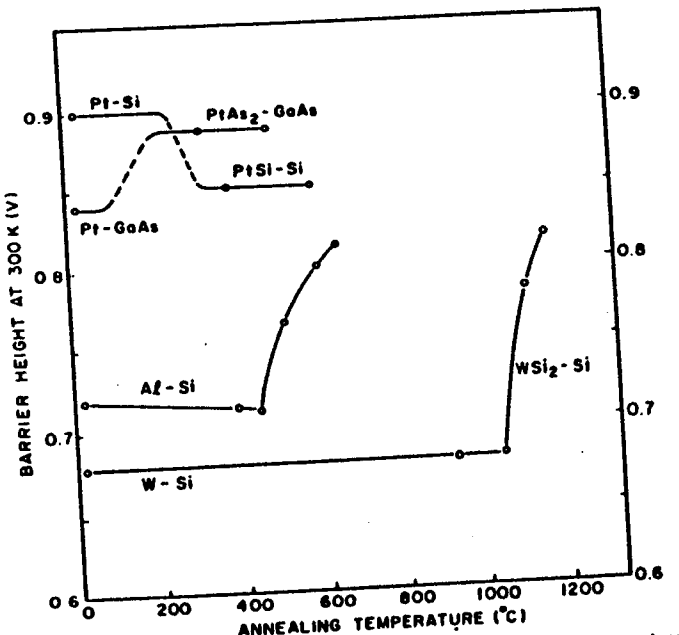

Fig. 33 Barrier heights on *n*-type Si and GaAs measured at room temperature after annealing at various temperatures.

pre-deposition and post-deposition heat treatments.[44] Figure 33 shows the barrier heights on *n*-type Si and GaAs measured at room temperature after annealing at various temperatures. The barrier height of a Pt–Si diode is 0.9 V. After annealing at 300°C or higher temperatures, PtSi is formed at the interface[45] and ϕ_{Bn} decreases to 0.85 V. For Pt–GaAs contact the barrier height increases from 0.84 V to 0.87 V when $PtAs_2$ is formed at the interface.[46] When an Al–Si diode is annealed above 450°C, the barrier height begins to increase[47] presumably due to diffusion of Si in Al (also see Fig. 27). For a W–Si diode the barrier height remains constant until the annealing temperature is above 1000°C, where WSi_2 is formed.[48]

5.5.3 Barrier Height Adjustment

For a standard Schottky barrier, the barrier height is determined primarily by the character of the metal and the metal–semiconductor interface property and is nearly independent of the doping. Usual Schottky barriers on a given semiconductor (e.g., *n*- or *p*-type Si) therefore give a finite number of choices for barrier height (Tables 3 and 4).

GOOD EXAMPLE OF SEMI-CONDUCTOR LAB REPORT

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Current-Voltage (I-V) and Capacitance-Voltage (C-V) Characteristics of $Au/Bi_4Ti_3O_{12}/SnO_2$ Structures

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ABSTRACT

The electrical properties of $Au/Bi_4Ti_3O_{12}/SnO_2$ structures were investigated by forward bias I-V, forward and reverse bias C-V and G/ω-V measurements. The results indicate structural disordering, presence of the interface states in the BTO capacitors and existence of polarization. Dielectric constant(ε'), dielectric loss(ε") and dielectric tangent(tanδ) were found as 170, 309 and 1,8 respectively at 50 kHz. C-V and G/ω-V were measured in the frequency range of 1 kHz-5 MHz. It was found that dielectric constant(ε') and dielectric loss(ε") systematically decrease with increasing frequency in 10 kHz-1 MHz frequency range and tanδ versus frequency plot exhibits a minimum at about 5 kHz. The ideality factor and series resistance were found to be 1,5 and 1030 Ω respectively from I-V measurements and series resistance was found as 350 Ω from the measured conductance in strong accumulation region. The observations are comparable with the other values for BTO structures reported in the literature.

Key Words: $Au/Bi_4Ti_3O_{12}/SnO_2$ structures, Dielectric constant, Dielectric loss, Frequency dependence, Series resistance

1. INTRODUCTION

When a metal is brought into intimate contact with a semiconductor, a potential barrier is formed at the metal- semiconductor (MS) interface [1]. In 1938, Schottky suggested that the rectifying behavior could arise from a potential barrier as a result of the stable space charges in the semiconductor. This model is known as the Schottky Barrier (SB). Metal-semiconductor devices can also show non-rectifying behavior; that is, the contact has a negligible resistance regardless of the polarity of the applied voltage. Such a contact is called an ohmic contact. The height of potential barrier can be determined by the difference between the work function of the metal (Φ_m) and semiconductor (Φ_s) [1]. The work function is the energy difference between the vacuum level and Fermi level (E_F). When a forward bias voltage V_a is applied to the junction, the effective barrier height in the semiconductor becomes q (Φ_B-V_a) and the electron flow from the semiconductor into the metal is enhanced by a factor, exp(qV_a/kT). Experimentally obtained barrier heights deviate from this rule and the basic mechanisms of the Schottky Barrier formation are still a field of intensive research. $Bi_4Ti_3O_{12}$ structures are the simplest and among the most well known compounds among the bismuth layer-structured ferroelectrics and are particularly interesting because of their peculiar switching behavior [2,3] resulting from a small c-axis component of the spontaneous polarization and a small coercive force. $Bi_4Ti_3O_{12}$ is a typical ferroelectric material with useful properties.

2. MATERIAL AND METHODS

The $Bi_4Ti_3O_{12}$ (BTO) thin film which is used in this study was obtained through hot compaction of $Bi_4Ti_3O_{12}$ powder. The mixture of Ar and O_2 was used as a working medium. The structure of the obtained BTO thin film was determined by rf magnetron sputtering. The BTO thin film was grown on SnO_2 substrate. The chemical composition of film was determined by the X-ray energy dispersive spectroscopy method using a scanning electron microscope REM-101M. The spectral line intensity relation for BTO films was compared with a standard sample. After composing the back ohmic contact, the gold top contacts (rectifying contacts), with a thickness of about 2000 Å and a diameter of 2.5 μm, were deposited on the films by using a shadow-mask at room temperature by rf sputtering. The electron diffraction patterns of $Bi_4Ti_3O_{12}$ film with a thickness of ~2 μm were obtained by magnetron sputtering on crystal substrate at

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temperatures around 700 °C. The measurements of capacitance vs. voltage (C-V) and conductance vs. voltage (G-V) characteristics for the $Au/Bi_4Ti_3O_{12}/SnO_2$ structure were performed by using a Hewlett-Packard HP 4192 A LF impedance analyser (5 Hz-13 MHz) at various frequencies between 1 kHz and 5 MHz. The current-voltage (I-V) characteristics for $Au/Bi_4Ti_3O_{12}/SnO_2$ structure were obtained by using a Keithley model 614 electrometer and 220 programmable constant current source at room temperature. The sample was mounted on a copper holder in a box and the electrical contacts were created with the upper gold electrodes by using tiny silver coated wires with silver paste.

2.1. Current-Voltage Characteristics

A typical forward bias semi-logarithmic ln(I)-V characteristics of $Au/Bi_4Ti_3O_{12}/SnO_2$ structures is shown in Figure 1. The ln(I)-V curve consists of two linear regions with different slopes, one at low bias ≤0,7 V and one at mid bias region (0,7V≤V≤ 0,9V) showing the exponential relationship between the current and voltage.

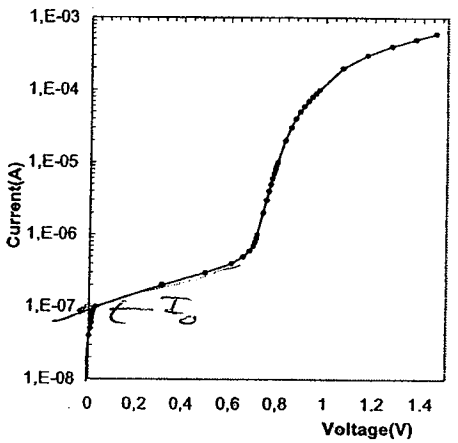

Figure 1. Forward bias I-V characteristics of $Au/Bi_4Ti_3O_{12}/SnO_2$ structures.

In high bias region (≥ 0,9 V) the series resistance R_s can be dominated from linear part. The most interesting region for a Schottky diode, i.e., the mid bias region which is dominated by the diffusion component of the current, shows a linear behaviour in the semi-logarithmic plot enabling one to extract the important diode parameters (ideality factor n, reserve saturation current I_s and barrier height). The most common theory of Schottky barrier diode is based on the thermionic emission (TE) and according to this model, the current-voltage (I-V) relationship is given by;

$$I = I_S\left[\exp\left(\frac{qV_B}{kT}\right)-1\right] \quad (1)$$

where q is the electronic charge, k is the Boltzman constant, T is the absolute temperature, V_B is the voltage across the junction and I_S is the reserve saturation current and described by [1],

$$I_S = AA^*T^2\exp\left(-q\phi_B/kT\right) \quad (2)$$

where A is the area of rectifying contact (diode), A^* is the modified Richardson constant and ϕ_B is the effective barrier height from metal to semiconductor. The I_S was found as $6{,}13.10^{-15}$ Amphere by extrapolating the linear mid bias region of the curve to zero applied voltage axis and the ideality factor n was found to be 1,5 from the slope of this linear region. When the structure has a series resistance and interface states, ideality factor n becomes higher than unity; most practical Schottky diodes show deviation from the ideal thermionic theory. For the case of the diode with a high series resistance and ideality factor, the relation between the applied forward bias V and the current I can be written as [10-13],

$$I = I_S\exp\left[\frac{q}{kT}\left(V - IR_S\right)\right] \quad (3)$$

when $V_D > 3kT/q$ [1]. A method to extract the series resistance R_s of ideal Schottky diode (i.e., n=1) was first proposed by Norde [10]. For 1<n<2 case, Sato and Yasamura [11] and n>>1 case Bohlin [12] modified Norde's approach to extract the values of n, R_S and ϕ_B from the forward bias I-V data of any Schottky diode. The equation can be written as:

$$V = R_S AI + n\phi_B + n\frac{kT}{q}Ln\left(I/AA^*T^2\right) \quad (4)$$

Differentiating Eq.(4) with respect to I and rearranging the terms,

$$\frac{d(V)}{dLn(I)} = n\left(\frac{kT}{q}\right) + R_S I \quad (5a)$$

$$H(I) = V - \left(n/\beta\right)\ln\left(I/AA^*T^2\right) = n\phi_B + R_s I \quad (5b)$$

can be obtained [13]. Thus, a plot of d(V)/dln(I) vs I will give R_s as the slope and n(kT/q) as the y-axis intercept. At room temperature the d(V)/dln(I) vs. I plot for $Au/Bi_4Ti_3O_{12}/SnO_2$ structure is shown in Figure 2 (a). The values of ideality factor n and series resistance R_s were found as 1,5 and 1030 Ω respectively. As can be seen, the values determined for the ideality factor n, obtained from the plots, are incompatible with each other.

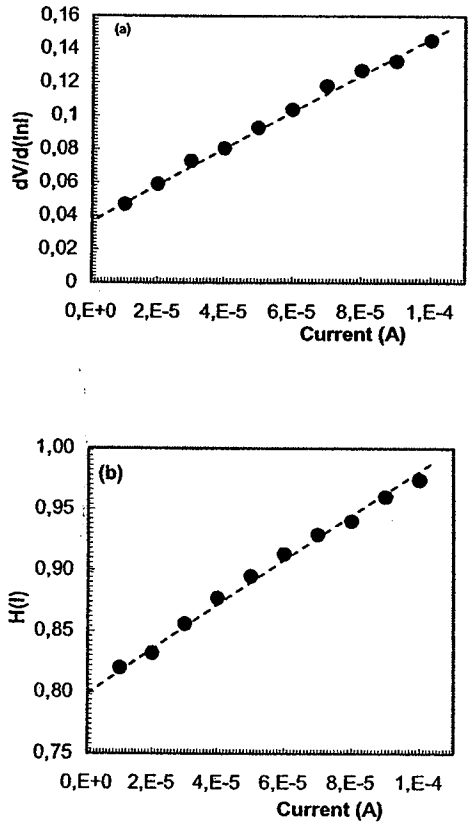

Figure 2. The experimental dV/d(lnI) vs. I and H(I)vs.plots for $Au/Bi_4Ti_3O_{12}/SnO_2$ structure.

Using the n value determined from Eq.(5a), H(I) vs. I plot will also give a straight line (Figure 2b) with y-axis intercept equal to $n\phi_B$. The slope of this plot also provides a second determination for R_s, which can be used to check the consistency of this approach. A departure from the linearity in ln(I)-V characteristics at high forward bias ($V \geq 0.9$ V) is usual and attributed to interface states and the series resistance of device[14,1].

2.2. Capacitance -Voltage Characteristics

With the top and bottom metal electrodes, the parameters of the Schottky diode, including the depletion layer capacitance (C_i), built-in voltage (V_{bi}) and space charge density (N_D or N_A) can be determined from a plot of $1/C_m$ (C_m is the measured capacitance) versus d_m (d_m is measured thickness), at various bias voltages. In this section we will show our calculations to determine the built in voltage V_{bi}, space charge density N_D, series resistance R_s and frequency dependence of dielectric constant (ε'), dielectric loss (ε'') and dielectric tangent ($\tan\delta$) quantitatively by using C-V and G/ω-V measurements and a detailed equivalent circuit analysis of BTO structures.

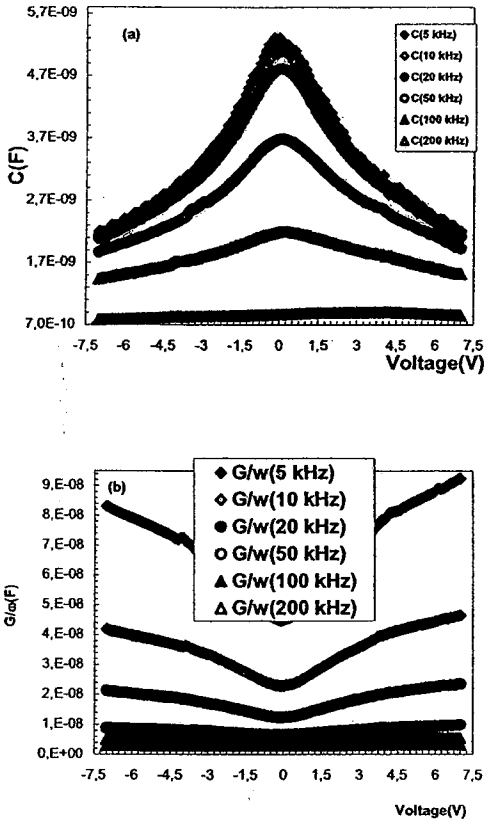

Figure 3. Measured capacitance(C) and conductance(G/ω) vs. gate bias for $Au/Bi_4Ti_3O_{12}/SnO_2$ at different frequency.

Figures 3(a) and 3(b) shows typical C-V, and G/ω-V curves of the structure whose BTO layer has a thickness d is 2 μm, at different frequencies (5 kHz -200 kHz). Additionally, the figures indicate the C-V-f and G/ω-V-f response for the Schottky diode, showing that the measured capacitance (C) and conductance (G/ω) are dependent on bias voltage and frequency. The voltage and frequency dependence is a function of a Schottky barrier; interface state density and high series resistance [16]. In Figure 4(b), the series resistance versus frequency curves show that at high frequency ($f \geq 100$ kHz) the series resistance of the diode decreases with increasing frequency. Figures 4(a) and (b) confirmed that the series resistance varies with applied bias and frequency. Here we assumed that Schottky barriers were formed at the top and bottom interfaces [11,13]. With built in voltage V_{bi}, a depletion width should follow a relationship such that

$$W_D = \left[\frac{2\varepsilon_i\varepsilon_o}{qN_D}(V_{bi} - V)\right]^{1/2} \quad (6)$$

where N_D, is the donor density, ε_i is the relative permitivity of interfacial layer and ε_o is the permitivity of vacuum [1].

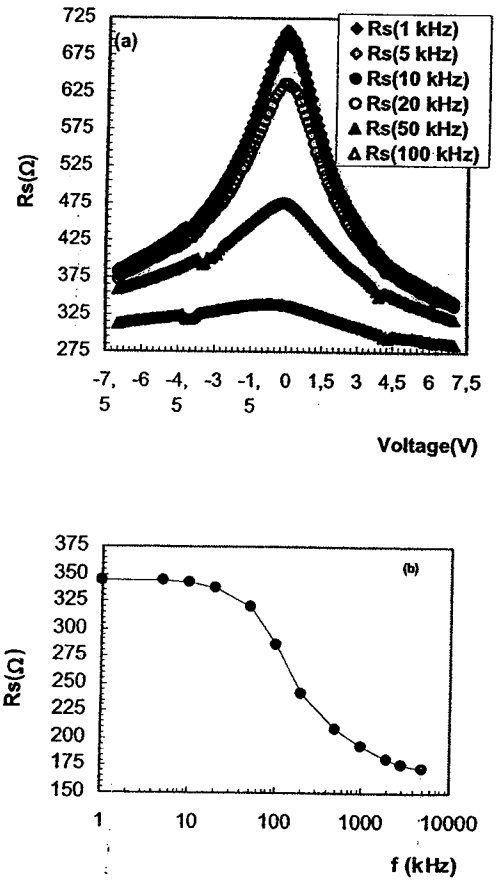

Figure 4. Frequency dependence of series resistance(Rs) for $Au/Bi_4Ti_3O_{12}/SnO_2$ structure.

It is known that a capacitance of a Schottky diode [1] can be represented by:

$$\frac{1}{C_m^2} = \frac{2(V_{bi} - V_i)}{q\varepsilon_s\varepsilon_o N_D A^2} \quad (7)$$

where V_i represents a drop of an external voltage at the interface of the capasitor when an external voltage is applied. The Eq.7 predicts a linear relationship between ($1/C^2$) and V under strong bias conditions. The carrier doping density (N_D) values used in the calculations were determined from the slope of the linear part plot of C^{-2} vs. V curves (Figure 5).

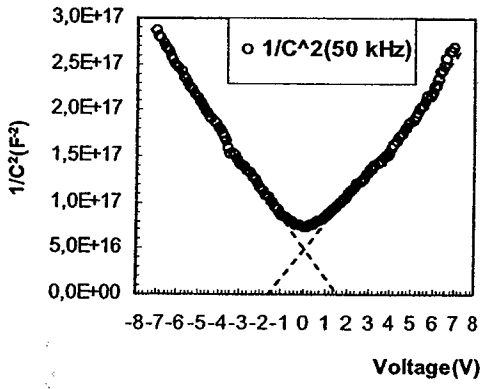

Figure 5. Plot of $1/C^2$ vs V for BTO structure at frequency of 50 kHz.

In 50 kHz frequency and at room temperature N_D value was found in the range of $1{,}36 \times 10^{15}$ cm^{-3}. The built in voltages of the BTO structure is cowed and obtained by fitting the high field with linear lines. From the x-axis (voltage) intercepts, it was found that V_{bi}=1,6 Volt. Additionally, series resistance can be calculated from the measured admittance (C-V and G-V) when the devices are based in a strong accumulation region according to [17]:

$$R_S = \frac{G_m}{G_m^2 + (\omega^2 C_m^2)} \quad (8)$$

where G_m and C_m represent equivalent parallel conductance and capacitance in the strong accumulation (at 6 volt) for the measured device. The series resistance is calculated ~350 Ω from the C-V and G-V curves in the strong accumulation bias. This value is higher than that of obtained from d(V)/dln(I) vs. I plot because I-V measurement was carried out only under forward bias conditions.

Additionally ε', ε" and tanδ were obtained at various frequencies, as shown in Figure 6. Dielectric constant ε' decreases with increasing frequency above 20 kHz. The measured small signal ε', ε" and tanδ were found to be 170, 309 and 1,8 respectively at 50 kHz. These observations are comparable to the reported values for BTO structures [18-22].

3. RESULTS AND DISCUSSION

A small signal of 40 mV amplitude and 50 kHz frequency was applied to the bias across the sample while bias was swung between -7 V and +7V. There was a decrease in the capacitance at strong bias and this reduction in the capacitance may be attributed to increased conductivity at strong dc bias. The dielectric constant (ε'), dielectric loss (ε") and dielectric tangent (tanδ) at frequency 50 kHz were found to be 170, 309 and 1,8 respectively. Frequency response for dielectric

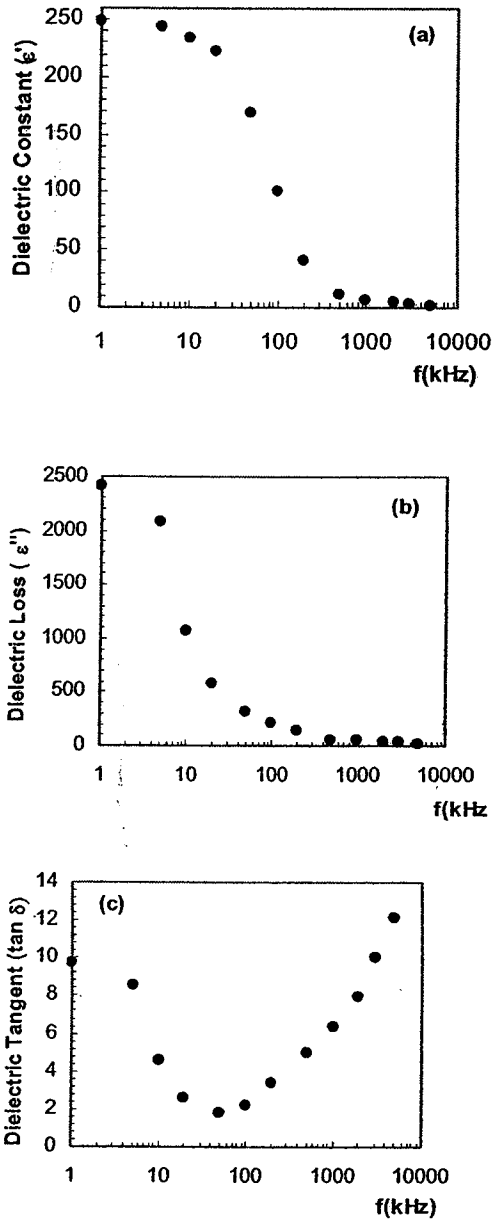

Figure 6. Dielectric constant, loss and tangent as a function of the frequency for $Au/Bi_4Ti_3O_{12}/SnO_2$.

properties, C-V and G/ω-V of $Au/Bi_4Ti_3O_{12}/SnO_2$ structures were measured in the frequency range of 1 kHz-5 MHz. While dielectric constant(ε') and dielectric loss (ε") decrease with increasing frequency, in the 10 kHz-5MHz frequency range, show a minimum at about 5 kHz. The ideality factor n and series resistance R_s were found at room temperature to be 1,5 and 1030 Ω respectively in forward bias I-V measurement. Additionally series resistance R_s was found to be 350Ω from the measured conductance in the strong accumulation region. The higher value of the ideality factor n and the dielectric constant (ε') may be attributed to a structural disorder of the structure, and also indicates the thickness of the structure layer and surface charge density. C-V-f and G/ω-V-f measurements confirmed that the measured capacitance C and conductance G strongly depend on applied bias voltage and frequency. This dependence is due to the presence of Schottky barrier, doping concentration (N_A or N_D), density of interface states (D_{it}) and series resistance (R_s). These observations are comparable to the reported values for BTO structures.

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REFERENCES

[1] Sze, S. M., "Physics of Semiconductor Devices 2nd ed.", ***John Wiley & Sons***, New York, 362-390 (1981).

[2] Cummins, S.E., "A new bistable ferroelectric light gate or display element", ***Proc. IEEE***, 55: 1537-1538 (1967).

[3] Cummins, S. E., Cross L. E., "Crystal symmetry, optical properties, and ferroelectric polarization of $Bi_4Ti_3O_{12}$ single crystals", ***Appl. Phys. Letters***, 10: 14-16 (1967).

[4] Wu, S.Y., Takei, W.J. , Francoma, M.H., "Transient switching response and partial switching phenomena in coarse-grained rhombohedral-phase PLZT ceramics", ***Ferroelectrics***, 10: 43-46 (1976).

[5] Agasiyev, A. A., Mamedov, M.Z., Muradov, M. B., "Electrical Conductivity and Dielectric Properties of $Bi_4Ti_3O_{12}$", ***J. Phys. III France***, 6 (7): 853-861 (1996).

[6] B.H., Park, S. J., Hyun, "Imprint failures and asymmetric electrical properties induced by thermal processes in epitaxial $Bi_4Ti_3O_{12}$ thin films", ***Journal of Applied Physics***, 84: 4428-4435 (1998).

[7] Joshi, P.C., Krupanidh, S.B., "Structural and electrical studies on rapid thermally processed ferroelectric $Bi_4Ti_3O_{12}$ thin films by metalloorganic solution deposition", ***Journal of Applied Physics***, 72 (12): 5817-5819 (1992).

[8] Pintilie, L., Pintilie, I., Petre, D., Botila, T., Alexe M., "Trap characterization of $Bi_4Ti_3O_{12}$ thin films by thermally stimulated currents", ***Appl. Physica A***, 69: 105-109 (1999).

[9] Fu, L., Liu, K., Zhang, B., Chu, J., "Capacitance-voltage characteristics of $Bi_4Ti_3O_{12}$/p-Si interface", ***Appl. Phys. Letters***, 72 (14): 1784-1786 (1998).

[10] Norde, H., "A modified forward I-V plot for Schottky diodes with high series resistance", ***Journal of Applied Physics***, 50 (7): 5052-5053 (1979).

[11] Sato, K., Yasamura, Y., "Study of forward I-V plot for Schottky diodes with high series resistance", ***J.Appl.Phys.***, 58 (9): 3655-3657 (1985).

[12] Bohlin, K.E., "Generalized Norde plot including determination of the ideality factor", ***J.Appl.Phys.***, 60 (3): 1223-1224 (1986).

[13] Cheung, S.K., Cheung, N.W., "Extraction of Schottky diode parameters from forward current-voltage characteristics", ***Appl.Phys. Lett.***, 49 (2): 85-87 (1986).

[14] Green, M.A., King, F.D., Shewchun, J., "Minority Carrier MIS Tunnel Diodes and their Application to Electron and Photovoltaic Energy Conversion Part I: Theory", ***Solid-State Electronics***, 17: 551-561 (1974).

[15] Özdemir, S., Altındal, Ş., "Temperature dependent electrical characteristics of Al-SiOx-pSi solar cells", ***Solar Energy Materials and Solar Cells***, 32 (2): 115-127 (1994).

[16] W. P., Kang, J. L., Davidson, Y., Gurbuz, D. V., Kerns, "Temperature Dependence and Effect of Series Resistance on Electrical Characteristics of a Polycrystalline Diamond MIS Diode", ***Journal of Applied Physics***, 78 (2): 1101-1107 (1995).

[17] Nicollian, E.H., Brews, J.R., "Metal Oxide Semiconductor (MOS) Physics and Technology", ***John Wiley & Sons***, New York, 423–491 (1982).

[18] Kong, L. B., Ma, J., "Randomly oriented Bi4Ti3O12 thin films derived from a hybrid sol-gel process", ***Thin Solid Films***, 379: 89-93 (2000).

[19] Wang, H., Fu, L. W., Hang, S. X., "Preparation and Properties of $Bi_4Ti_3O_{12}$ Single-Crystal Thin Films by Atmospheric Pressure Metalorganic Chemical Vapor Deposition", ***J. Appl. Phys.***, 73 (11): 7963 (1993).

[20] Joshi, P.C., Krupandihi, S.B., "Switching, fatigue, and retention in ferroelectric $Bi_4Ti_3O_{12}$ thin films", ***Appl.Phys. Lett.***, 62 (16): 1928-1930 (1993).

[21] A.Q., Jiang, G.H., Li,, L.D., Zhang, "Dielectric study in nanocrystalline $Bi_4Ti_3O_{12}$ prepared by chemical coprecipitation", ***J.Appl.Phys.***, 83 (9): 4878-4883 (1998).

[22] Lee, J.J., Alluri, P., Dey, S.K., "Effect of interfaces on the electrical behavior of (Pb0.72La 0.28) TiO3 thin films", ***Appl.Phys.Lett.***, 65 (16): 2027-2029 (1994).